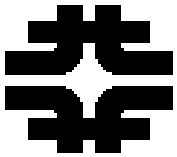

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Tevatron

Ion Profile Monitor (IPM) Clock System Hardware Manual

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1. Design Overview

Figure 1-1 is a block diagram of the Ion Profile Monitor (IPM) Clock PCI card. The card was designed to reside in a computer's standard PCI slot. The main function of the IPM Clock card is to provide a QIE clock and marker signals to the IPM front end electronics. The clock and marker signals are decoded from the raw tevatron TVBS and APTVBS encoded clocks. The phase and delay of the clock and marker signals are programmable through the PCI interface.

TVBS is received on a LEMO connector at the back panel of the computer. This 1/7 RF encoded clock is fed through a Phase Frequency Detector (PFD) and is filtered by an op amp to produce a control voltage on a 53.1047MHz VCXO, thus locking in phase to the TVBS. The 53MHz signal is a recovered clock that has no encoding on it and is used as a reference for a PLL multiplier. The multiplier is programmed to produce a phase adjusted 8/7 RF (8TVBS) that is fed back to the FPGA decoder. The FPGA contains a state machine that decodes PROTON MARKER and PROTON INJECTION TAG from the TVBS using the synchronized 8TVBS as its clock. A 2/7 RF QIE CLOCK is also generated from the 8TVBS. Similarly, the APTVS is decoded and ANTIPROTON MARKER and ANTIPROTON INJECTION TAG are produced. QIE CLOCK and the marker signals are then sent down to the front end electronics using differential PECL and standard network-type RJ45 connectors and straight through UTP5 cable. There are two unique output channels (A and B) that contain identical clock and timing signals but have separate phase and delay programming capability.

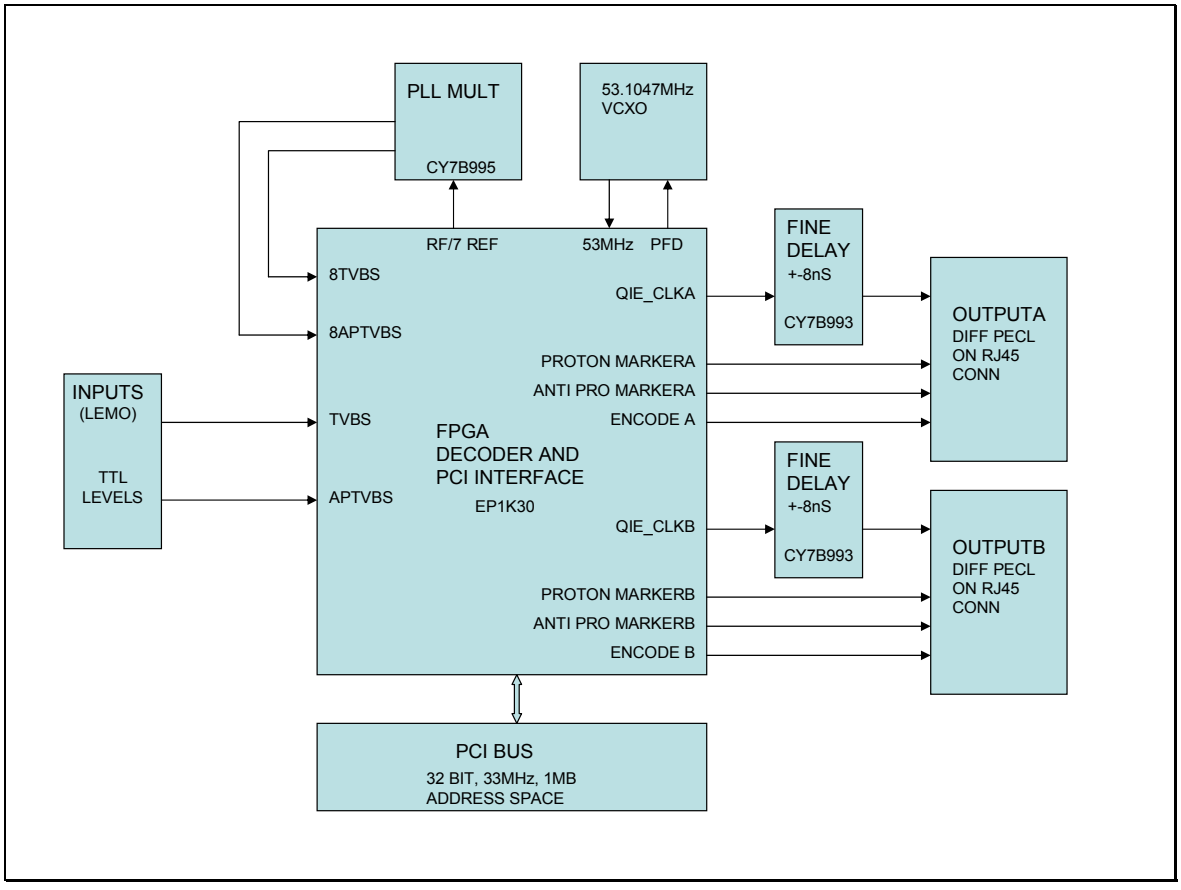

Figure 1-1 – IPM CLOCK CARD BLOCK DIAGRAM

2. PC Board Physical Layout Overview

The IPM clock card is designed to reside in a free 32 bit PCI slot of any standard personal computer. The PCI connector was notched to fit in a 5V or 3.3V PCI slot. Figure 1-2 is a picture of the IPM Clock card. To the left are the rear panel input/output connectors. TVBS and APTVBS are TTL level signals received on standard right angle LEMO connectors. The signals are terminated into 50 ohms and buffered by a 74LVT125. These encoded clocks are passed along to the Atera ACEX1K FPGA in the middle of the card. A phase detector circuit and VCXO are placed to the upper right of the FPGA. The circuit locks on to the TVBS phase and produces a stable RF clock for the card. A 1/7 RF reference is fed to the Cypress CY7B995 multi-phase clock buffer/multiplier. Two phase aligned multi-phase buffer outputs at 8/7 RF frequency are fed back to the FPGA for use in decoding TVBS and APTVBS. The FPGA outputs QIE CLK (2/7 RF), Proton Marker, Antiproton Marker, and an encoded bit to the IPM front end electronics via the RJ45 output connectors. The Cypress CY7B994V multi-phase buffers to the left of the FPGA are used to adjust the phase of the QIE CLKA and QIE CLKB outputs. MAX9370 TTL to PECL translators to the left of the CY7B994s are used to drive the 200 foot CAT5 UTP cables. The FPGA code is held in the ALTERA EPC2 configuration device to the lower right of the FPGA. The EPC2 is downloaded via a standard JTAG 10 pin header and an ALTERA Byteblaster cable. A TI 73HD325 regulator to the right of the FPGA provides the 2.5V FPGA core voltage and power on reset.

Figure 2-1 – IPM CLOCK CARD PICTURE

3. PCI Interface, Memory Map, and Register Function

The PCI interface for the IPM Clock card is implemented in the ACEX1K FPGA using an ALTERA IP core. The specific core used is the “pci_t32”, a target only, 32-bit, 33MHz device. Figure 1-3 outlines the registers and control functions contained within the 1MB of PCI address space allocated to the clock card. The actual base address is unique to each installation. The address space listed below is the offset from the base address.

Bar0 Offset	Function Name	valid data	Function Description
0x00	CSR0	D[7..0]	Control Status Register (write 8 bits, read 24 bits)
0x04	CLKA DELAY	D[5..0]	CLKA delay in 64 steps of 1.029nS
0x08	CLKB DELAY	D[5..0]	CLKB delay in 64 steps of 1.029nS
0x0C	PROTON MARKERA DELAY	D[8..0]	PRO MARKER A delay in 317 steps of 132nS
0x10	PROTON MARKERB DELAY	D[8..0]	PRO MARKER B delay in 317 steps of 132nS
0x14	ANTIPROTON MARKERA DEL	D[8..0]	ANTIPRO MARKER A delay in 317 steps of 132nS
0x18	ANTIPROTON MARKERB DEL	D[8..0]	ANTIPRO MARKER B delay in 317 steps of 132nS
0x1C	TVBS PHASE ADJUST	D[2..0]	TVBS fine phase adjustment for decoding
0x20	APTVBS PHASE ADJUST	D[2..0]	APTVBS fine phase adjustment for decoding
0x24	APTVBS COARSE ADJUST	D[3..0]	APTVBS coarse phase adjustment for decoding
0x28	CLKA_CONTROL	D[2..0]	Send commands to front end
0x2c	CLKB_CONTROL	D[2..0]	Send commands to front end
0x80	SOFTWARE RESET	N/A	Reset latched errors

Figure 3-1 – PCI Memory Map

3.1. CSR0 Description

Control/Status Register (CSR0, 0x00) is a general purpose register used to enable/disable functions and read pertinent status from the card. Currently most of this register is used for status, as shown in figure 3-2 below.

CSR0 BIT	Function	CSR0 bit function description
0	MODE	0 = TVBS decode mode, 1 = local timing
6..1	RESERVED	
7	ERROR CHECK ENABLE	0 = Error Checking Off, 1 = Error Checking On
8	TVBS LOCK STATUS	1 = TVBS PLL LOCKED
9	CLKA LOCK STATUS	1 = CLKA PLL LOCKED
10	CLKB LOCK STATUS	1 = CLKB PLL LOCKED
11	RESERVED	
12	TVBS LOCK ERROR	1 = TVBS PLL LOCK ERROR (WHEN CSR0[7] = 1)
13	CLKA LOCK ERROR	1 = CLKA PLL LOCK ERROR (WHEN CSR0[7] = 1)
14	CLKB LOCK ERROR	1 = CLKB PLL LOCK ERROR (WHEN CSR0[7] = 1)
15	RESERVED	
16	PROTON MARK A MISSING	1 = PROTON MARK A MISSING (CSR0[7] = 1)
17	PROTON MARK B MISSING	1 = PROTON MARK B MISSING (CSR0[7] = 1)
18	AP MARK A MISSING	1 = AP MARK A MISSING (WHEN CSR0[7] = 1)
19	AP MARK B MISSING	1 = AP MARK B MISSING (WHEN CSR0[7] = 1)
23..20	FPGA VERSION NUMBER	HIGHER NUMBER IS MORE RECENT VERSION

Figure 3-2 – CSR0 Function Bit Map

3.1.1. CSR0 Control Bit Functions

There are two control functions associated with CSR0. Bit 0 = 0 is the normal running mode where clock and timing are derived from TVBS and APTVBS. Bit0 = 1 is a local mode, where clock and timing are based solely on the free running 53MHz VCXO and internal counters.

Bits 1-6 are reserved and can be written/read but have no function.

Bit 7 = 1 enables the error checking features of the card. The default power on setting of bit 7 is zero. This is because the all of the errors would upon power up due to PLL and VCXO lock times.

3.1.2. CSR0 Status Bit definitions

Status bits 8-23 are read only bits. Bits 8-10 are the lock status of the three multi-phase PLL buffers on the board. These bits should always be 1. A constant zero on any of these bits indicates a clock problem.

Bits 12-14 monitor the lock status of the PLLs on a more dynamic basis. An intermittent or constant locking problem will be latched by these errors. A software reset must be issued to clear these error flags.

Bits 16-19 monitor the revolution marker decoding on TVBS and APTVBS. Once these markers have been decoded for the first time after power up, they should be present on every revolution. If a marker is not detected at the expected periodic interval, an error is latched. Reasons for this error include PLL locking problems, input cable intermittent, or state machine decoding errors. A recurring latched marker missing error indicates a problem with the card or cabling.

Bits 20-23 are a fixed four bit number corresponding to the FPGA firmware version number.

3.2. Clock Delay Registers (CLKA Delay, CLKB Delay)

The two clock delay registers (0x04, 0x08) are 6 bit write/read registers that control the phase of the QIE Clock by delaying the recovered clock in steps of 1.029nS. The 6 bits represents 64 unique settings that span one full 2RF/7 QIE Clock cycle (65.9nS). The markers and other timing signals will follow these phase changes if they are latched with the rising edge of the QIE Clock in the front end.

3.3. Marker Delay Registers (Proton Marker Delay, Antiproton Marker Delay)

The four marker delay registers (0x0C, 0x10, 0x14, 0x18) are 9 bit write/read registers that delay the markers to the front ends in 317 steps of 132nS. This represents almost one full Tevatron turn of 2RF/7 clock cycles. One complete turn is 318 2RF/7 cycles. The marker delays are necessary to align the marker with beam arrival time in the front ends. Note that setting a delay register above 317 will result in loss of or unpredictable marker signal behaviour.

3.4. Encoded Clock Input Phase Adjust (TVBS Phase Adjust, APTVBS Phase Adjust)

Two write/read phase adjust registers (0x1C, 0x20) of 3 bits are used to adjust the phase of the 8TVBS and 8APTVBS clocks so that reliable decoding is achieved. This is an expert adjustment made once for a particular installation after all the hardware is in place. If the source of TVBS/APTVBS changes or the length of the LEMO input cable changes, this phase should be checked. The adjustment is made while looking at 8TVBS vs. TVBS (or 8APTVBS vs. APTVBS) on an oscilloscope. The phase of 8TVBS should be adjusted so that the falling edge of 8TVBS is coincident with the rising edge of TVBS. This relationship yields a good setup/hold time for the decoding state machines.

3.5. APTVBS Coarse Input Phase Adjust (APTVBS Coarse Adjust)

A 4 bit write/read register at offset 0x24 is used to adjust the phase of the Antiproton markers to match the phase of the Proton Markers. This phase adjustment is implemented as a delay of 264nS (16 steps of 16.4nS). Since the phase of the input APTVBS is unknown with respect to the TVBS phase and the 8RF/7 is derived from TVBS, a delay that spans more than one RF/7 period is necessary to align APTVBS with all possible phases of TVBS. This adjustment should only have to be made once during setup, either with an oscilloscope comparing proton and antiproton marker outputs, or empirically using front end data.

3.6. Clock Control (CLKA_CONTROL,CLKB_CONTROL)

The clock control (0x28,0x2C) feature of the IPM clock board sends commands to the front ends utilizing an encoded single bit scheme. These commands are not timing critical and can be serialized into one bit to allow use of a standard 8 conductor category 5 cable (The other 3 pairs are used by QIE_CLK, PROTON_MARKER, and ANTI_PROTON MARKER). Figure 3-3 outlines the 4 control bit definitions.

Bits 0-1 choose one of four possible front end data taking modes while bit 2 set to one instructs the encoded bit state machine to send a change mode command to the front end. Bit 2 returns to zero when the mode change command is complete. Writing a one to bit 3 initiates a front end QIE reset. The bit returns to zero when the reset command is complete.

CLKA/B CONTROL BITS		**CSR0 bit function description**
1..0	MODE	CHOOSES ONE OF FOUR MODES
2	CHANGE MODE	1 = CHANGE MODE, READS 0 WHEN DONE
3	QIE RESET	1 = QIE RESET, READS 0 WHEN DONE

Figure 3-3 – Clock Control Bit Definitions

Figure 3-4 outlines the encoded bit definitions. The encoded bit is normally low in its inactive state. Encoded patterns are clocked on the rising edge of QIE_CLK, with an approximate setup time of 30nS and hold of 35nS. The start of an encoded pattern is defined by two consecutive "ones". The three subsequent latched bits define one of eight possible encoded commands as shown in the table below. The most significant bit arrives first.

binary code	**pattern definition**
000	undefined, null
001	Proton Injection Tag
010	Antiproton Injection Tag
011	Change to Mode 0
100	Change to Mode 1
101	Change to Mode 2
110	Change to Mode 3
111	QIE Reset

Figure 3-4 – Encoded Bit Definitions

Figure 3-5 is a Quartus II simulation snapshot of an example encoded clock sequence. In this example, a PCI write to the appropriate register initiated a change mode and QIE reset sequence. Since Change Mode is a higher priority, this command is sent first. Immediately following is the QIE reset. The "QIE_CLKA" and "ENCODE_A" are the actual outputs sent to the front end boards.

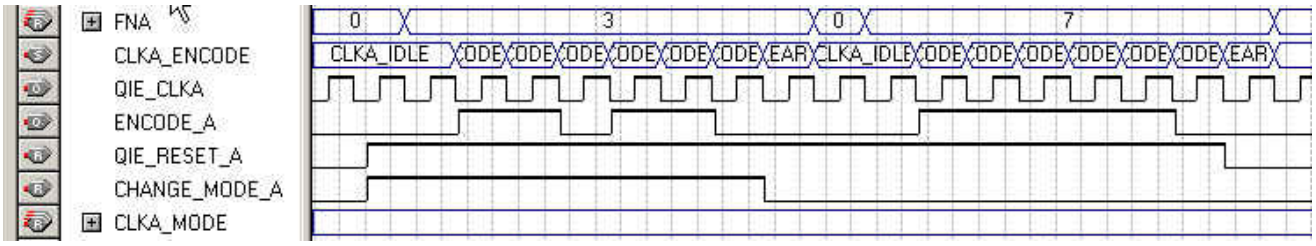

Figure 3-5 – Encoded Bit Sequence Simulation

3.7. Software Reset (0x80)

The software reset command is issued when a write to address 0x80 is executed. The data sent is ignored. There is no read function at this address. Software Reset returns state machines to their idle state and clears any latched errors.

4. Altera FPGA code

The Altera ACEX1K30 FPGA is the main logic device on the IPM Clock card. It handles the PCI interface, clock and timing decoding state machines, clock synchronization, encoded bit state machine, and all coarse delay functions. The code is written in the Altera Hardware Description Language (AHDL). The bulk of the code is defined and commented in the file http://www-ppd.fnal.gov/EEDOffice-w/Projects/Beams_Div/Beams_IPM_Clock/pci_local_target_clock.tdf. This file is best viewed within the Altera design environment but can be viewed using a standard text editor.