Beam Loss Monitor System Control Bus Testing

Summary of Bus Testing Efforts

October 10, 2005

BLM Control Bus Interface

- The BLM Control Bus is a custom bus structure that is incorporated into the BLM VME J2 Backplane. The Control Bus is an asynchronous, single master bus with an 8-bit wide data path and 13 address lines.
- Control lines are MREQ*, MRD* and MWR*. These bus control lines are active low. The Control Bus uses a split termination scheme identical to VME Bus. Inactive or Tri-stated bus lines are pulled to approximately 3 volts (logic one).

Initial Tests

- Al Baumbaugh wrote an Assembly Language test routine to verify the reliable operation of the BLM Control Bus.
- The test writes known (but different) data to 6 registers on the TC, 32 registers on the ACC, and 14 registers on each DC. The data is read back, compared with the known value that was written to that register and an error is logged if the values are different.
- This test routine was executed by the 48 MHz eZ80 on the BLM Controller card.

Initial Test Results

- Verified that the test would catch errors by removing a card while running the test.
- Assembly Language test routine for Control Bus ran on the BLM Controller card for about 14 hours.
- From 9/22 – 9/23 this test completed 803,143,680 cycles without errors.
- Each **test cycle** is 216 Control Bus operations. This is over 173 billion bus cycles without error.

A Quick Look at Signals

- This was a look at the quality of the Control Bus signals on the backplane. Trace (A1) is MREQ* and (A2) MWR*. Sampled at slot five, with full and no load in the VME crate.
- A full load consisted of 1 Timing Card, 1 Abort Controller Card, and 5 Digitizer Cards.
- No load in this case is defined as a single Timing Card. (This was the minimal amount of hardware required to allow the test to run without error.)

Control Bus Waveforms

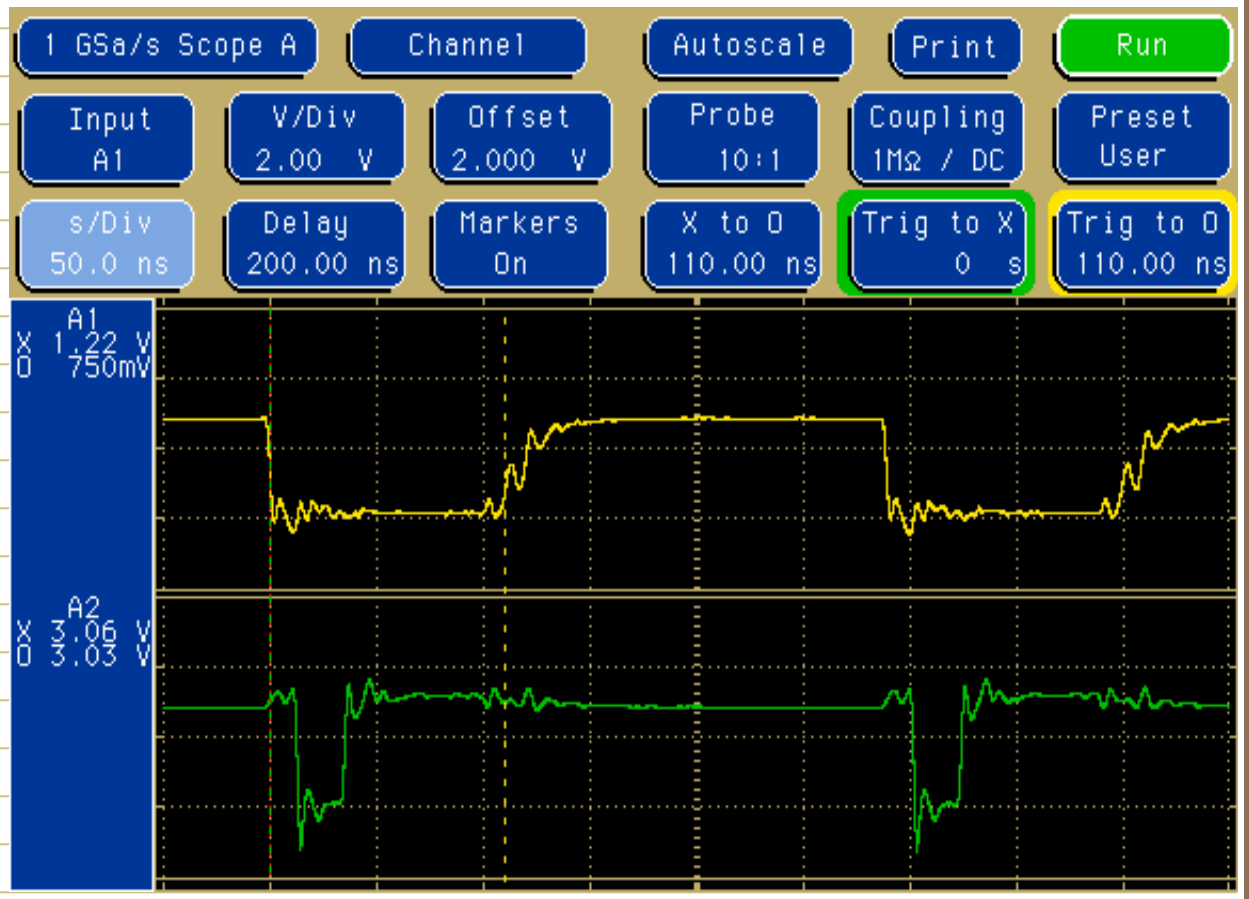
(Waveforms from VME crate slot 5, next to slot 4, the driving slot).

File Name:
CNTBFL05.TIF

Channel A1
MREQ* is (Yellow).

Channel A2
MWR* is (Green).

This is full load.



Control Bus Waveforms

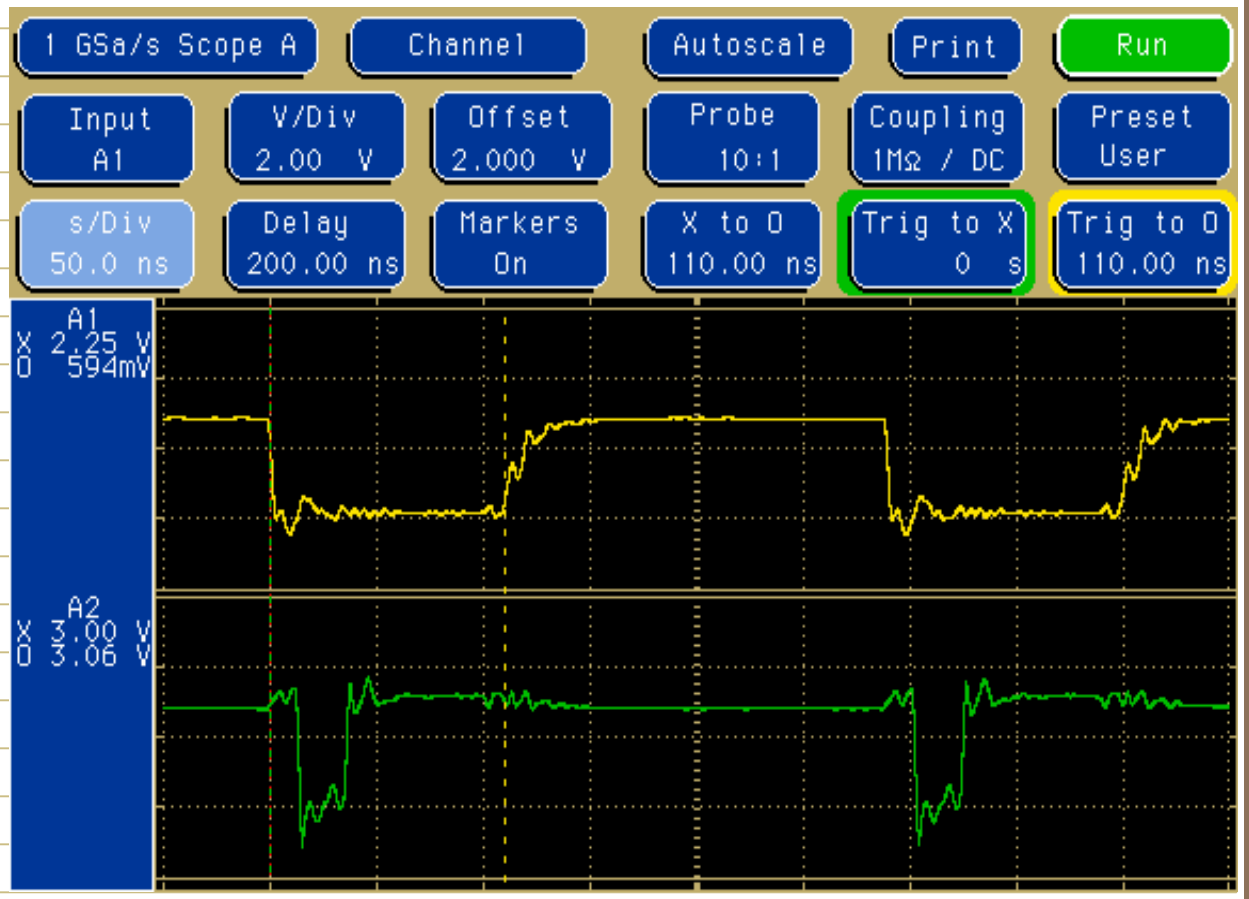
(Waveforms from VME crate slot 5, next to slot 4, the driving slot).

File Name:
CNTBNL05.TIF

Channel A1
MREQ* is (Yellow).

Channel A2
MWR* is (Green).

This is no load.



A Closer Look

- ⇨Need to look at the three main Control Bus signals (MREQ*, MRD*, MWR*) while running test.
- ⇨Check pulse width and rise time on MWR* at each end of the backplane.
- ⇨Possible to check MWR* with full load?
- ⇨Look at additional signals, if time.

MWR* Rise Time Measurements

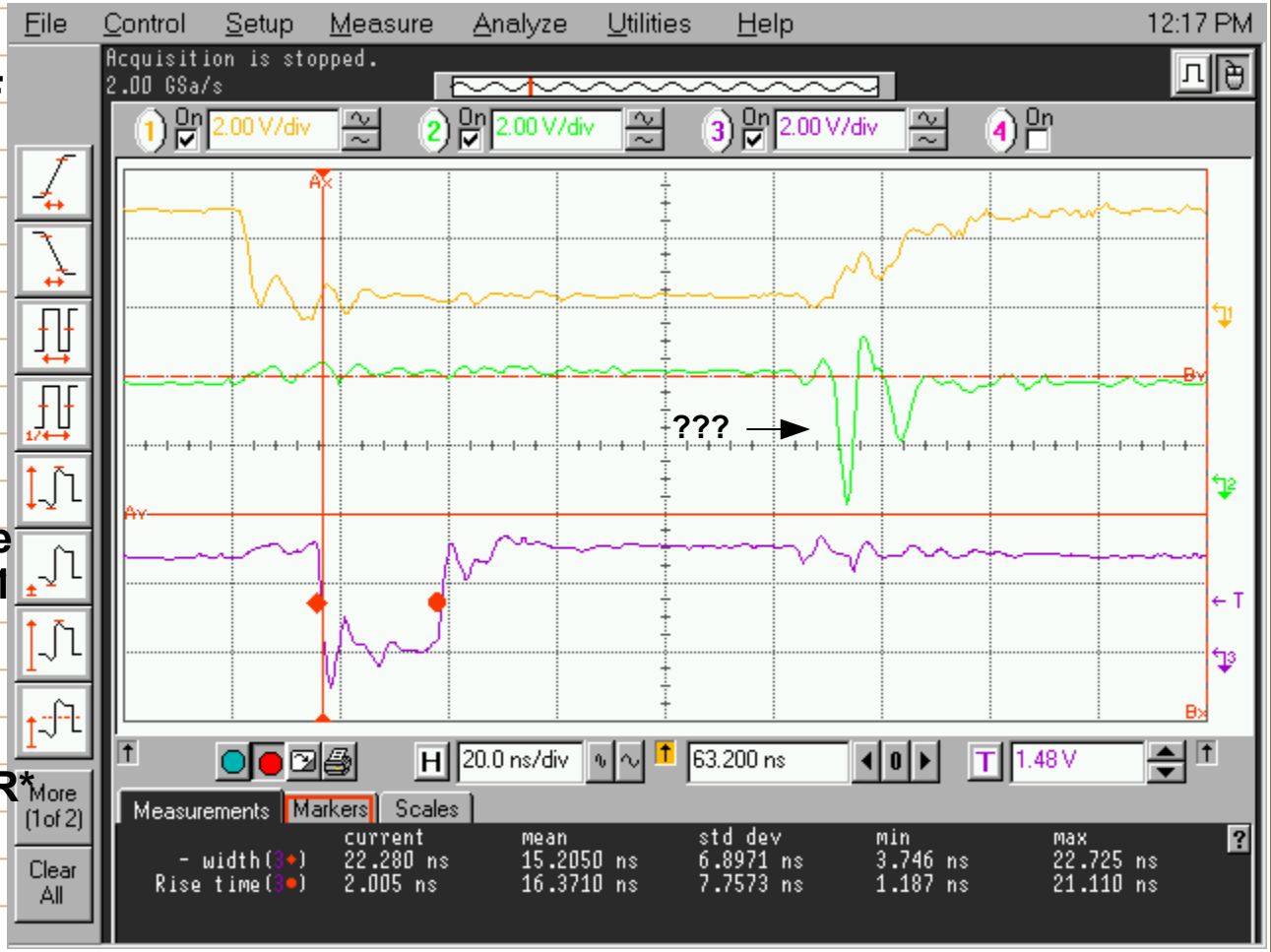
Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBWR05FLrs.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

View of:
Control Bus write cycle with 1 TC, 1 ACC, and 5 DC's as load.

Control Bus MWR* strobe width (22 ns) and rise time (2 ns) measured.



MWR* Rise Time Measurements

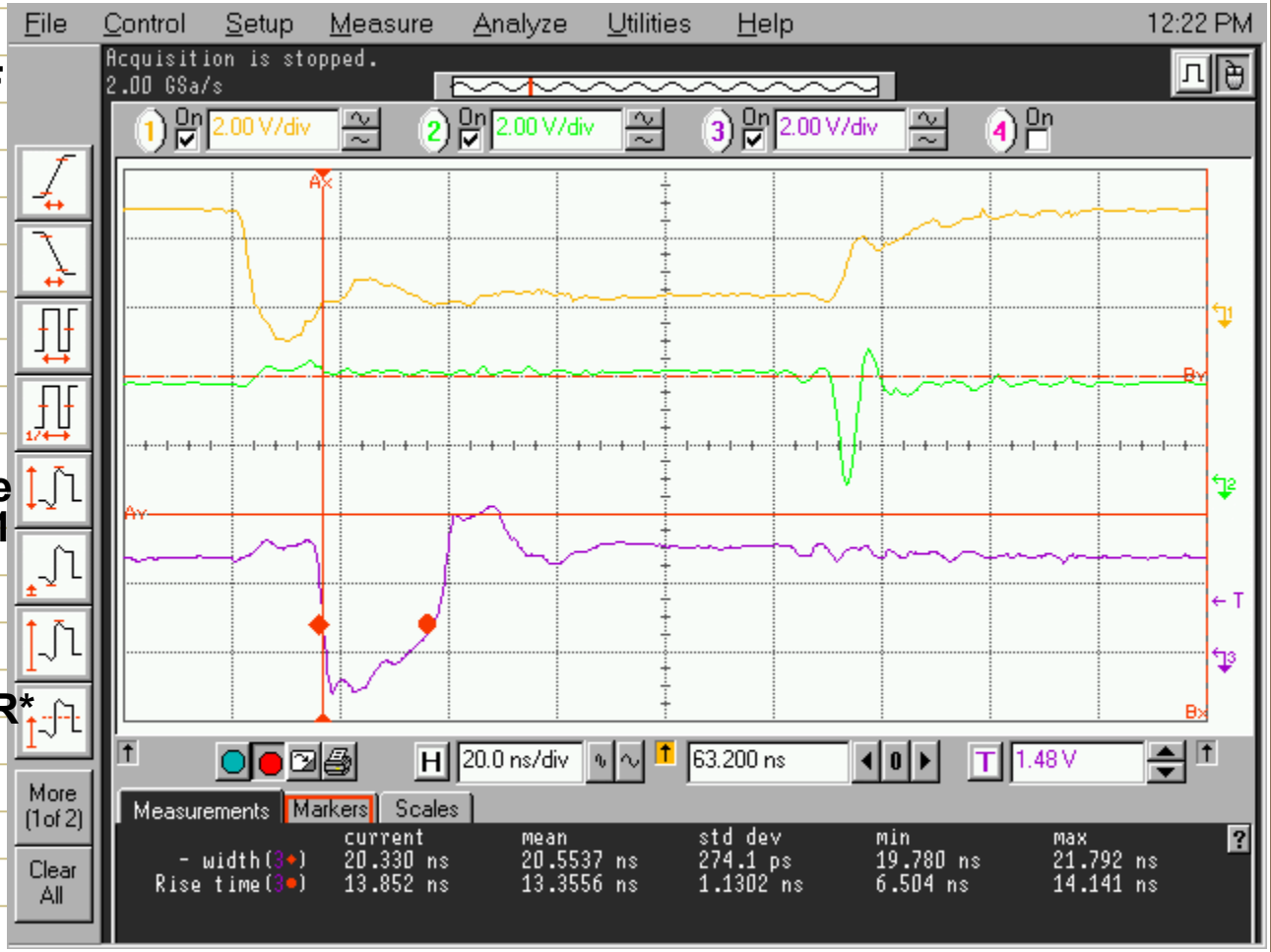
Signals Acquired at Slot 21 on Control Bus Backplane.

File Name:
CBWR21FLrs.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

View of:
Control Bus write cycle with 1 TC, 1 ACC, and 5 DC's as load.

Control Bus MWR* strobe width (20 ns) and rise time (13? ns) measured.



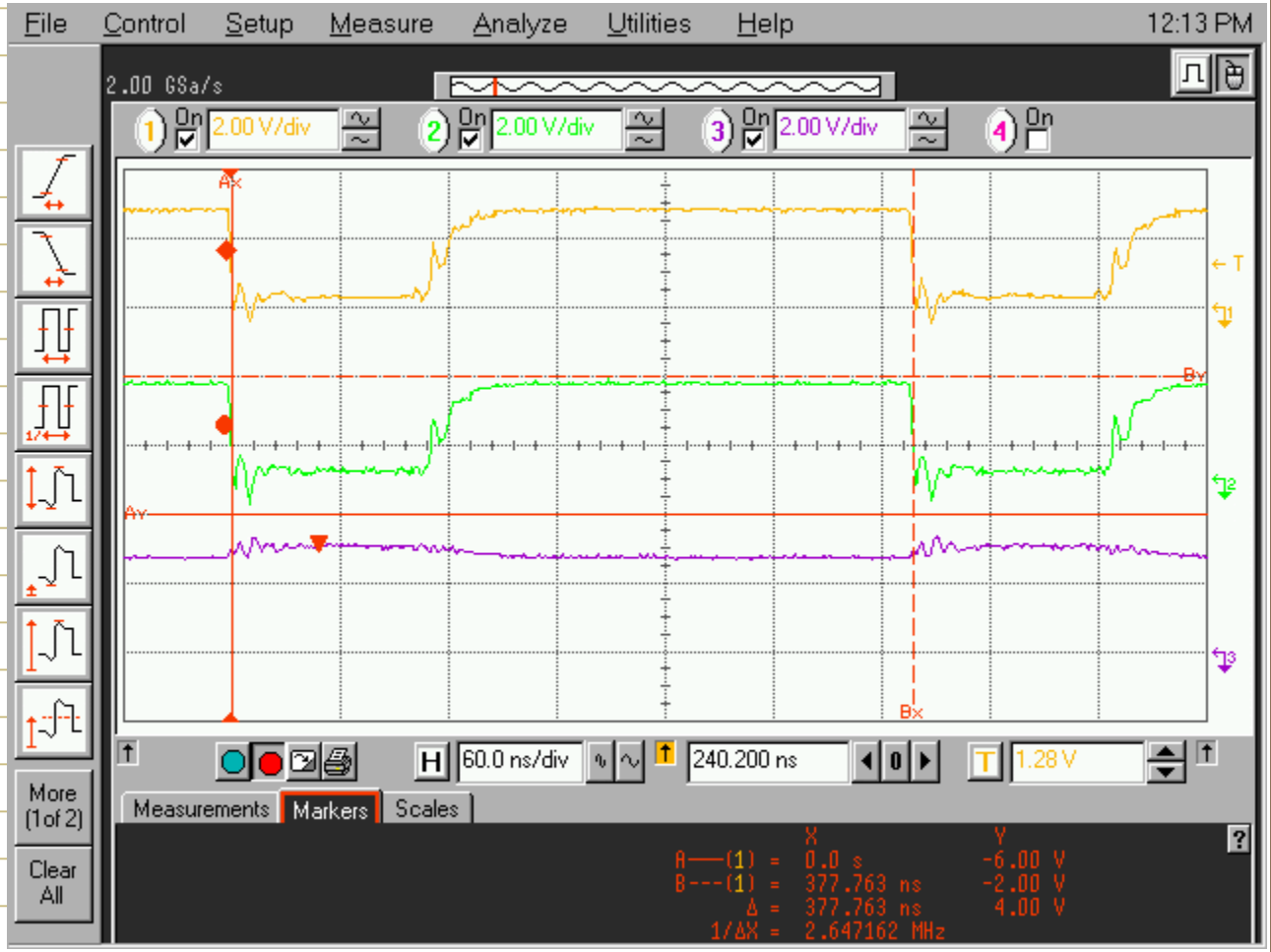
Multiple Read Bus Cycles

Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBRD05FLm.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

View of:
Multiple Control Bus read cycles.



10/01/2005

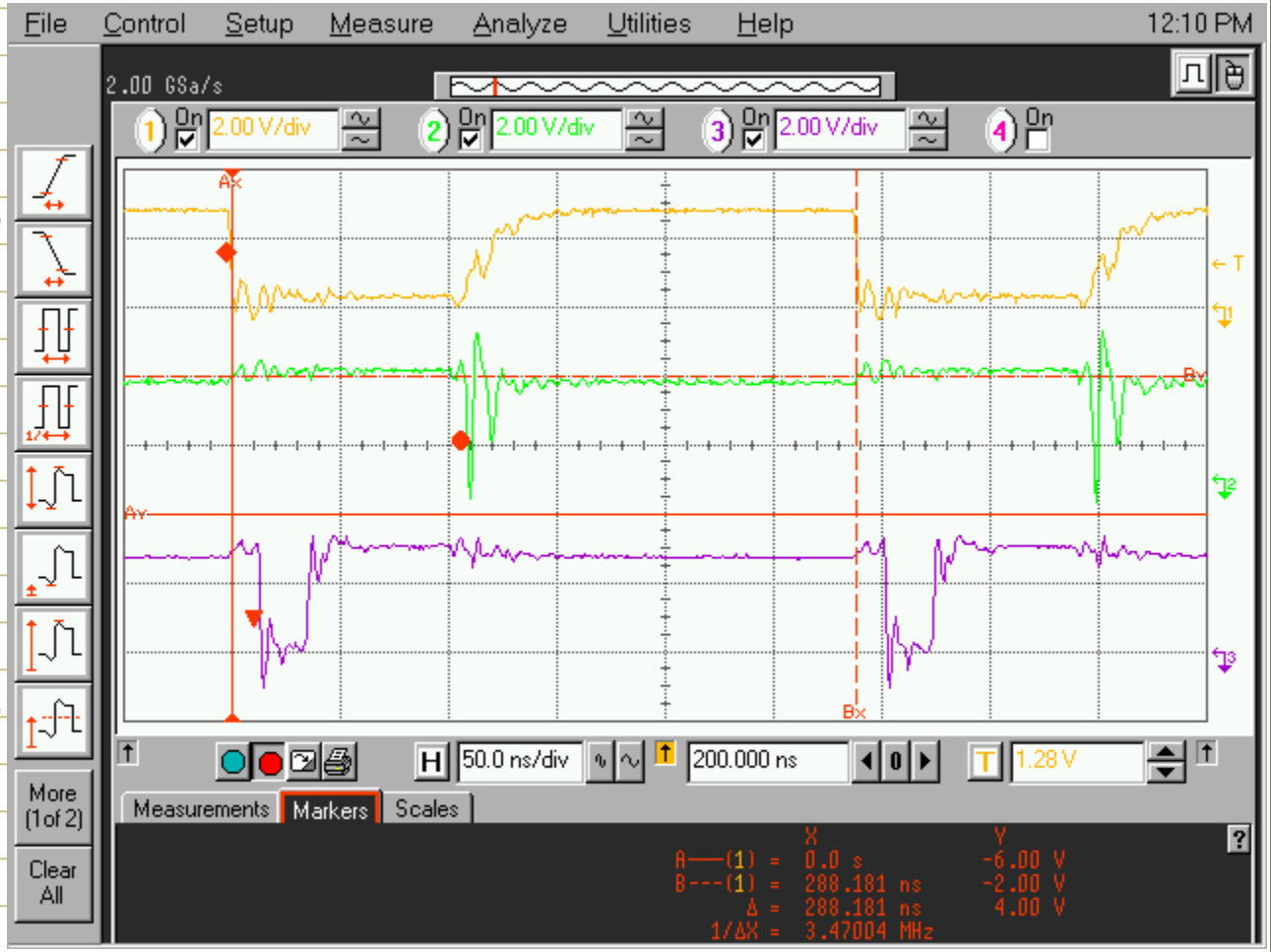
Multiple Write Bus Cycles

Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBWR05FLm.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

View of:
Multiple Control Bus write cycles.



Additional Load for Control Bus

- Would the test run successfully if the system had a full load of cards? How to simulate a heavily loaded system?
- Control Bus MWR* is critical as it is the signal with shortest pulse width (22ns).
- Load MWR* with additional capacitance.
- Control Bus slots 5-13 have a 15pf capacitor installed on A Row between pins 17 (MWR*) and 18 (GND)
- Additional load is: 9 x 15pf = 135pf
- VME spec. is: ≤ 20pf per slot (For Add/Data).

Additional Load for Control Bus

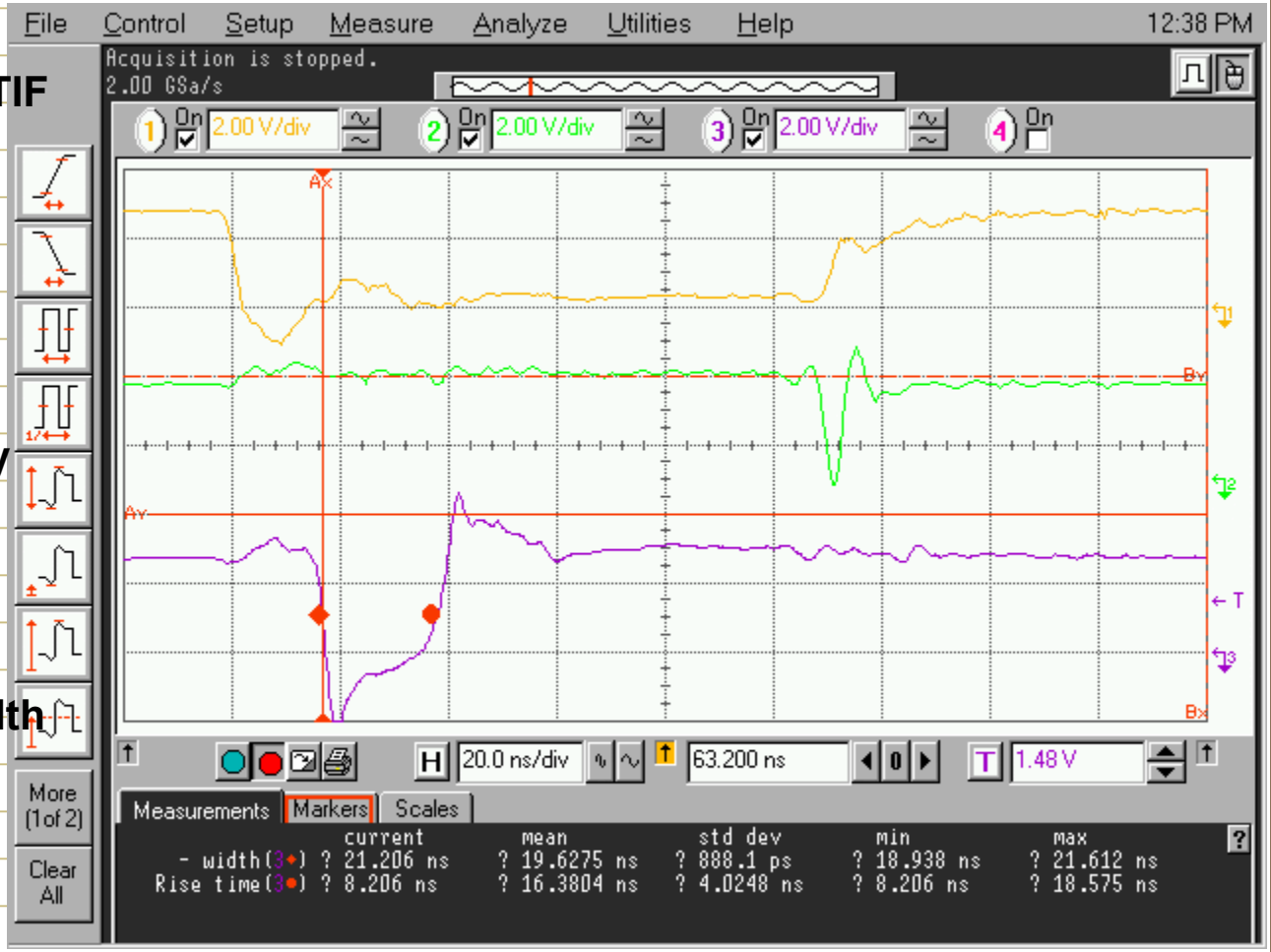
Signals Acquired at Slot 21 on Control Bus Backplane.

File Name:
CBWR21cap_rs.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

Simulating a fully loaded system.

View of:
Write cycle with MWR* strobe width and rise time measurements displayed.



Additional Load Test Results

- Test was run with a 1 TC, 1 ACC, 5 DC's, and a 15pf capacitor installed on slots 5 thru 13, loading MWR* with 135pf of additional capacitance.
- Test ran for 42,926,080 cycles with out error. (This is 9.27 Billion Control Bus operations.)

Full Load for Control Bus

- ⇨Would additional capacitance on MWR* cause the test to fail?
- ⇨Test is closer to a fully loaded system.
- ⇨Control Bus slots 5-19 have a 15pf capacitor installed on A Row between pins 17 (MWR*) and 18 (GND).
- ⇨The added load on MWR* is: 15 x 15pf = 225pf.

Full Load for Control Bus

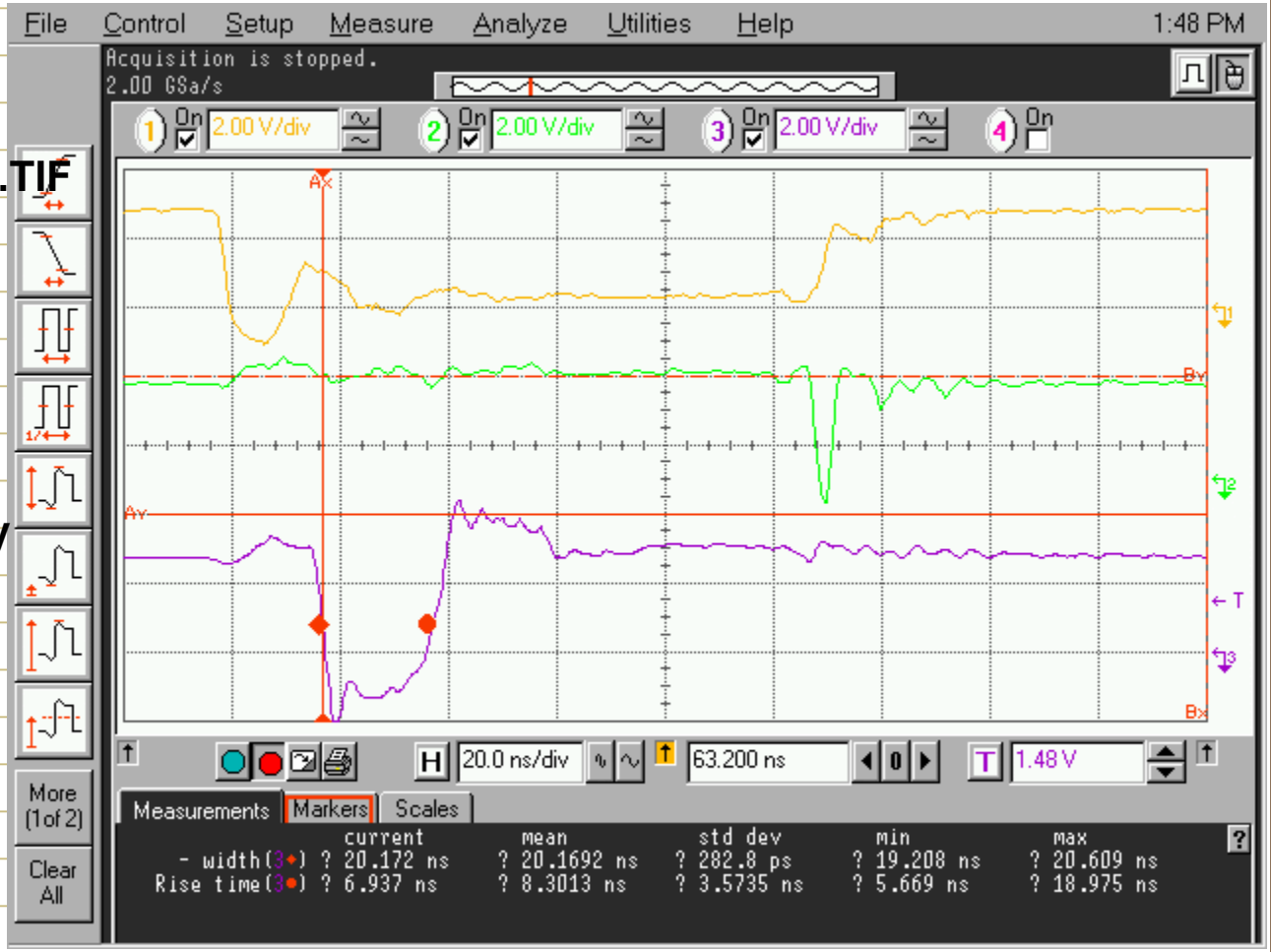
Signals Acquired at Slot 21 on Control Bus Backplane.

File Name:
CBWR21caps_rs.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

Simulating a fully loaded system.

Additional 15 pf caps on slots 14-19 and one card under test.



Full Load Test Results

- Test was run on individual cards with a 15pf capacitor installed on slots 5 thru 19, loading MWR* with 225pf of additional capacitance.
- **Card Test Results**
- TC ran for 16,711,680 cycles without error.
- AC ran for 16,384,000 cycles without error.
- DC ran for 13,565,952 cycles without error.
- All BLM cards ran without error. Test limited by length of available time.

Bus Bandwith Estimates

- In normal operation the BLM Controller Card will need to read out a maximum of 48 channels and a time stamp in 1 millisecond or less.
- Readout of a single channel is 4 bytes.
- Readout of the time stamp is 8 bytes.
- Total number of bytes to read is 200. (48 ch. x 4 bytes) + 8 bytes = 200

Bus Bandwith Estimates

- To complete the readout of all 48 channels and the time stamp (200 bytes) in the required 1 millisecond time frame, we have to be able to read a byte over the Control Bus every 5 microseconds.
- A short assembly language program was written to test the speed of consecutive Control Bus accesses.

Bus Bandwidth Measurement

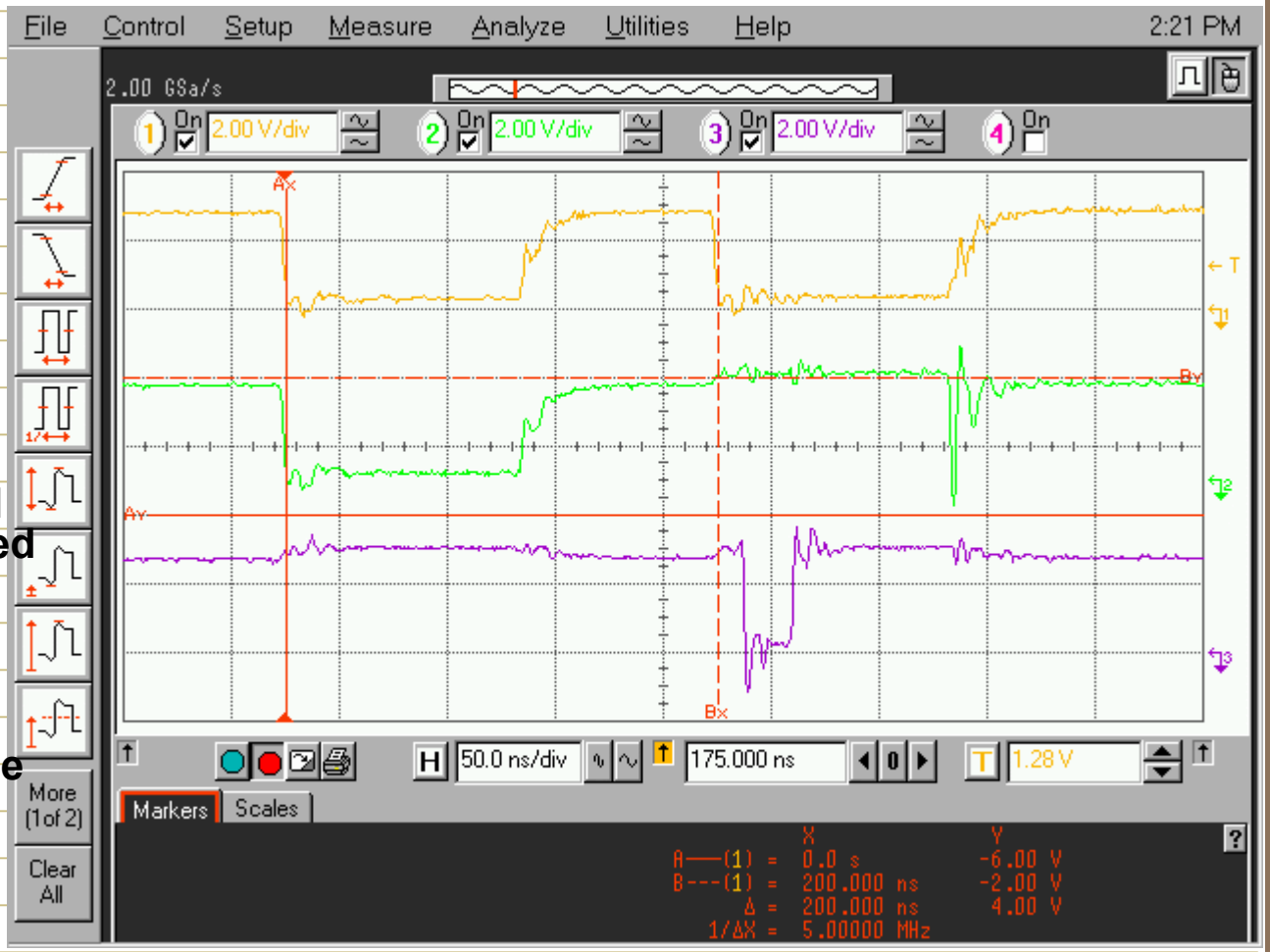
Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBRW05SPD.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

View of:
Control Bus read operation followed by a write.

Assembly language loop used to determine speed of consecutive bus cycles. (Cycles every 200ns.)



Bus Bandwidth Estimates

- Requirement: Need to read 200 bytes in a 1 millisecond time frame. This means reading a byte over the Control Bus every 5 microseconds. (200 KHz)
- Previous slide shows that it is possible to have a Control Bus read or write operation every 200 ns. (5 MHz)
- The Control Bus has 25 times the bandwidth necessary for BLM operations.

Control Bus Modifications

- As a result of the initial testing two modifications of the Control Bus were made.
- The FPGA firmware on the Controller Card was modified to remove glitch on the MRD* strobe when a write operation occurred. (See slides 9, 10, 12, etc.)
- To ease concerns about signal quality and timing issues the Control Bus MWR* strobe was lengthened to 44ns.

Modified Bus Waveforms

Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBRW05new.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)

A quick look at the modified Control Bus cycle.

Slide shows glitch free Control Bus write operation followed by a read. MWR* strobe is now 44ns wide.

10/07/2005

Address Bus Waveforms

Signals Acquired at Slot 5 on Control Bus Backplane.

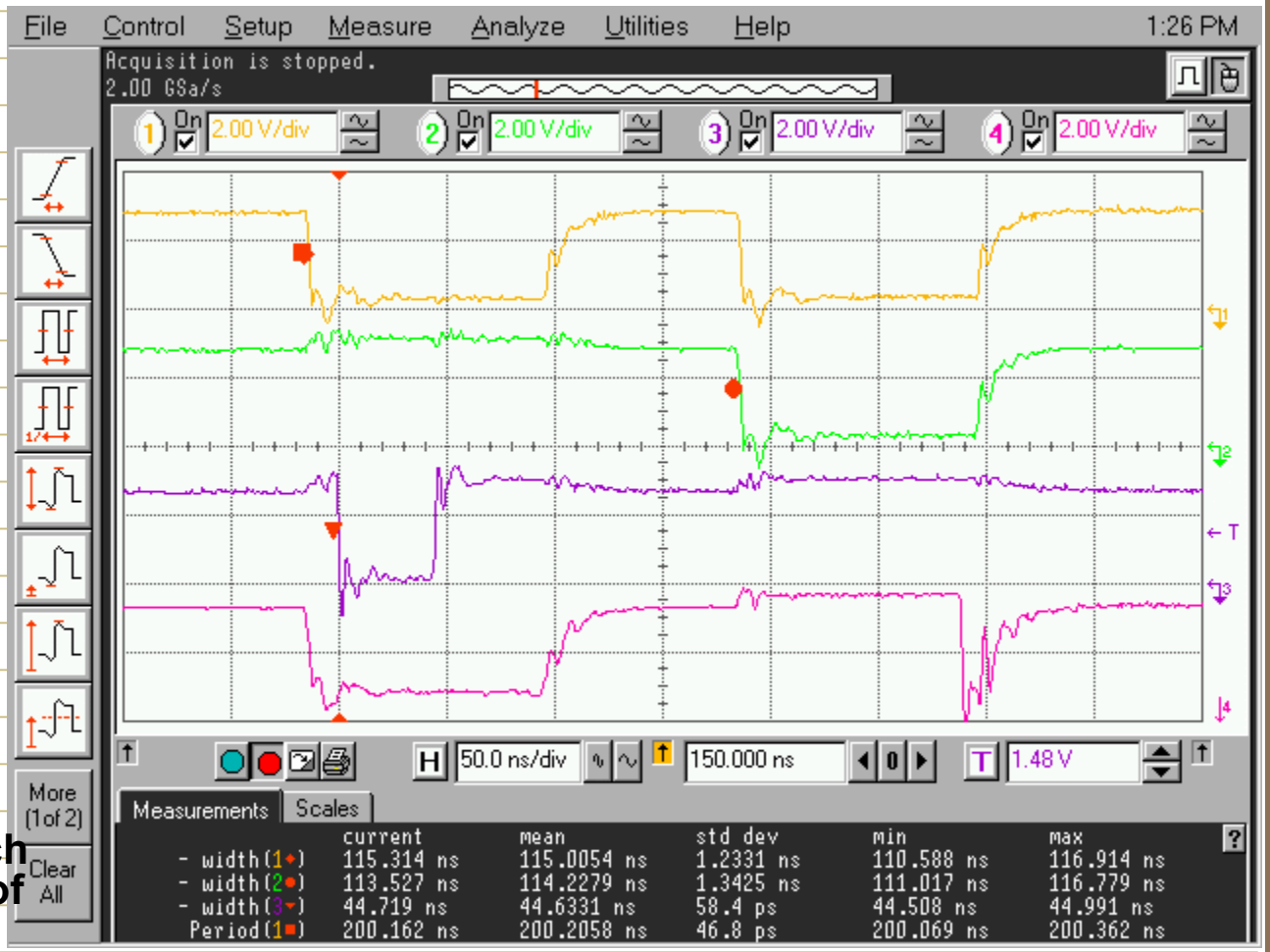
File Name:
CBRW05add.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)
ADD(0) (Pink)

Looking at the modified Control Bus cycle.

Test loop writes at address 0 and reads at 1.

Slide shows glitch on AD(0) at end of read cycle.



Address Bus Waveforms

Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBRW05add10.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)
ADD(0) (Pink)

View of:
The modified Control Bus cycle.

Test loop writes at address 1 and reads at 0.

Slide shows glitch on AD(0) at end of write cycle.

Data Bus Waveforms

Signals Acquired at Slot 5 on Control Bus Backplane.

File Name:
CBRW05add10.TIF

Signals:
MREQ* (Yellow)
MRD* (Green)
MWR* (Violet)
Data(0) (Pink)

View of:
The modified Control Bus cycle.

Test loop writes a data 0 and reads a 0.

Control Bus Testing Summary

- ⇨Control Bus bandwidth is 25 times greater than required.
- ⇨Controller Card FPGA firmware modified to remove glitch on MRD* strobe.
- ⇨Control Bus MWR* strobe width increased to 44 ns from 22 ns.
- ⇨Need to modify Controller Card FPGA firmware to remove glitch on address lines.