

TEL Vacuum Interlock

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Introduction

There are certain power supplies in the Tevatron Electron Lens (TEL) systems, both TEL1 and TEL2 that need to be disabled in the event of bad vacuum in the Tevatron. Two vacuum monitoring systems have been installed for both TEL machines to provide permit interlocking signals. Input signals to the interlock chassis are outputs of ion pump and vacuum gauge power supplies whose corresponding vacuum devices in the beam line are those that are located closest to the electron guns and collectors. Comparators in the interlock chassis monitor the ion pump power supply and ion gauge signals and disable the permit when vacuum is out of range. The permit signal is provided as both a TTL signal and a relay contact. The interlock chassis are connected to Ethernet for remote control and monitoring, and each interlock chassis utilizes an I.R.M. chassis as an ACNET front end. Table 1 lists the hardware physical locations and associated Ethernet assignments.

Each chassis has one ACNET parameter defined for the purpose of monitoring a trip condition and to provide the ability to reset it. Other defined parameters are for diagnostics and a level of control not necessarily required by the operations department.

The interlock chassis have input connectors for as many as 5 vacuum devices, although presently 3 are used for TEL1 and 4 are used for TEL2. The interlock circuits contain window comparators that monitor the input vacuum signals and sum the comparator conditions to generate the permit signals. The upper and lower limit values of the four window comparators are settable remotely. The last saved limit values are stored permanently in the interlock chassis. Note that the hardware and firmware for both TEL systems is configured the same; likewise ACNET parameters L1VAC and L2VAC. Channel 3 is jumpered to channel 4 on the front of the TEL1 interlock chassis at the present time for this system to work properly.

Window comparators are used for checking vacuum limits because the vacuum monitor signals out of the ion pump and ion gage power supplies have fault conditions at both high and low voltages. The vacuum signal voltage range is unipolar 0 to 10 V. When high voltage on the ion pump power supplies is turned off, the vacuum monitor output voltage goes up to about 9.8 V. Excellent vacuum is also a high voltage, but not as high as when the supply is off. Poor vacuum is a low voltage. At the low voltage end, the monitored voltage asymptotically approaches roughly 2.25 V for vacuum approaching 10^{-5} Torr and lower.

The hardware interlock circuitry is an assembly composed of two PCBs: a digital board and data acquisition board. The digital board implements the CEC protocol to communicate over Ethernet with an ACNET front end. Refer to Beams document 2109-V1 for the CEC protocol. Data arrays required for the CEC protocol to communicate with the interlock chassis are defined in this document.

Table 1: Ethernet assignments

		TEL1	TEL2
I.R.M. Front End	node name:	67D	67B
	IP address:	131.225.128.110	131.225.128.4
	Chassis location:	ZG5-ZRR-57	TG9-ZRR-103
Vacuum Interlock Chassis	domain name:	Tel1vacintlk.fnal.gov	Tel2vacintlk.fnal.gov
	IP address:	131.225.139.126	131.225.139.2
	local port:	4524	4524
	VLAN:	3	3
	Chassis location:	Relay rack A01-04	Relay rack A01-03

ACNET parameters and chassis functionality

The ACNET parameters defined for monitoring trip conditions and providing a reset are T:L1VAC and T:2VAC. These are defined in Table 2. These parameters also indicate which of the input channels was the first to trip out of range. Trip conditions are latched and must be manually reset by an operator before the interlocked TEL equipment will resume operation.

The remaining parameters provide the ability to set the trip limit values for the window comparators. These parameters are listed in Tables 3 and 4 which also shows which vacuum device is monitored by which input channel. Table 5 defines the properties for all the trip limit parameters. Their properties are all the same. Keep in mind though that for an upper trip limit, the input signal must go above the set voltage value to trip the permit. For a lower trip limit, the input must go below the set value.

There is one ACNET parameter for each trip limit. There are, therefore, two parameters associated with one input channel. The trip limit parameters display the vacuum of the device associated with it in the reading field. In the case of the readings, both limit parameters of a channel will display the same vacuum reading. The setting field displays the trip limit setting value and is settable. The trip limit settings are archived permanently in the interlock chassis and will independently return to the previous operating settings after a power outage or a power-on cycle.

The status field of each trip limit indicates whether it is tripped out of range high or low. In addition, if it was the first to trip in the chassis, its third status bit will indicate. All of the trip limit parameters have reset capability. Resetting any of the parameters will result in resetting all of the latches in the chassis.

The interlock chassis are always on. There is no way to remotely defeat the permit function. If one of the ion gauges is broken and is stuck with at either 0.0 or 10.24V, for example, about the only way to remedy the situation is to jumper two channels together at the input of the interlock chassis. Realize that it may be, then, necessary to change limit values of the jumpered channel.

Table2: T:L1VAC and T:L2VAC. TEL vacuum interlock trip and reset parameters.

Analog Properties	
Setting field:	none
Reading field:	none
Common units:	n/a
Primary units:	n/a
Digital Properties	
Status bit 1:	“.” (grn) – when there is no trip
	“1” (rd) – Vacuum channel #1 was the first of the four to have tripped out of range
Status bit 2:	“.” (grn) – when there is no trip
	“2” (rd) – Vacuum channel #2 was the first of the four to have tripped out of range
Status bit 3:	“.” (grn) – when there is no trip
	“3” (rd) – Vacuum channel #3 was the first of the four to have tripped out of range
Status bit 4:	“.” (grn) – when there is no trip
	“4” (rd) – Vacuum channel #4 was the first of the four to have tripped out of range
Reset Control Bit	This reset bit will reset all four vacuum channel comparator latches. (If the vacuum is still bad trip conditions will quickly reappear.)

Table 3: TEL1 vacuum interlock ACNET trip limit parameters.

ACNET Parameter	Trip Limit	Interlock Chassis Channel #	Vacuum Device
T:L1VM1U	upper	1	T:ATIG8A
T:L1VM1L	lower		
T:L1VM2U	upper	2	T:ATIG8B
T:L1VM2L	lower		
T:L1VM3U	upper	3	T:ATIP8M
T:L1VM3L	lower		
T:L1VM3U*	upper	4	T:ATIP8M*
T:L1VM3L*	lower		

* Redundant information. Channels 3 and 4 are jumpered together.

Table 4: TEL2 vacuum interlock ACNET trip limit parameters.

ACNET Parameter	Trip Limit	Interlock Chassis Channel #	Vacuum Device
T:L2VM1U	upper	1	T: A0IGTU
T:L2VM1L	lower		
T:L2VM2U	upper	2	T:A0IPTA
T:L2VM2L	lower		
T:L2VM3U	upper	3	T: A0IPTB
T:L2VM3L	lower		
T:L2VM4U	upper	4	T: A0IPTD
T:L2VM4L	lower		

Table 5: ACNET parameter properties for all upper and lower trip limit parameters.

Analog Properties	
Setting field:	Setting field is the trip limit setting—either upper or lower.
Reading field:	Reading field is the vacuum reading of the
Reading common units:	Primary units scaled to 0 – 10.24 V. Displayed units are “V”.
Reading primary units:	0x0000 – 0xFFFF 16-bit binary scaled to 0 – 10.24 V. Displayed units are “V”.
Digital Properties	
Status bit 1:	“.” (grn) – Vacuum voltage is not excessively high. “U” (rd) – Upper limit trip. Vacuum voltage is out of range--high.
Status bit 2:	“.” (grn) – Vacuum voltage is not excessively low. “L” (rd) – Lower limit trip. Vacuum voltage is out of range--low.
Status bit 3:	“.” (blank) “1” (rd) – This vacuum channel is the first to have tripped out of range.
Reset Control Bit	This reset bit will reset all four vacuum channel comparator latches. (If the vacuum is still bad trip conditions will quickly reappear.)

Ethernet communication between the interlock chassis and I.R.M. front end

The following information describes the structure of data exchanged between the interlock chassis and its ACNET front end per the CEC protocol as defined in the beams database document 2109-V1. This protocol requires data be organized into four arrays. The required arrays are described in Tables 6 through 9. The parameters listed under the ACNET Parameter column in the tables are those ACNET parameters utilizing the information of that particular data array element. ACNET parameters are constructed from the information contained in these four arrays.

The status array is defined in Table 8. There is one element of status for each vacuum channel. The bit assignment of each of the status array elements is the same and is described in Table 10.

Table 6: Type Code 0 – Array of analog readings.
Raw data range is 0x0000 – 0xFFFF

Element Number	Reading Description	TEL1 ACNET Parameter	TEL2 ACNET Parameter
0	Channel 1 vacuum	T:L1VM1U and T:L1VM1L	T:L2VM1U and T:L2VM1L
1	Channel 2 vacuum	T:L1VM2U and T:L1VM2L	T:L2VM2U and T:L2VM2L
2	Channel 3 vacuum	T:L1VM3U and T:L1VM3L	T:L2VM3U and T:L2VM3L
3	Channel 4 vacuum	n/a	T:L2VM4U and T:L2VM4L
4	Channel 5 (spare)	n/a	n/a

Table 7: Type Code 1 – Array of analog settings.
Raw data range is 0x0000 – 0xFFFF

Element Number	Setting Description	TEL1 ACNET Parameter	TEL2 ACNET Parameter
0	Chan 1 window comparator upper limit	T:L1VM1U	T:L2VM1U
1	Chan 1 window comparator lower limit	T:L1VM1L	T:L2VM1L
2	Chan 2 window comparator upper limit	T:L1VM2U	T:L2VM2U
3	Chan 2 window comparator lower limit	T:L1VM2L	T:L2VM2L
4	Chan 3 window comparator upper limit	T:L1VM3U	T:L2VM3U
5	Chan 3 window comparator lower limit	T:L1VM3L	T:L2VM3L
6	Chan 4 window comparator upper limit	n/a	T:L2VM4U
7	Chan 4 window comparator lower limit	n/a	T:L2VM4L
8	spare	n/a	n/a
9	spare	na/	na/

Table 8: Type Code 2 - Array of 16-bit Status words. Each element has 16 bits. See Table 10 for the bit assignments.

Element Number	Bit Description	TEL 1ACNET Parameter	TEL2 ACNET Parameter
0	Channel 1 status	T:L1VAC, T:L1VM1U and T:L1VM1L	T:L2VAC, T:L2VM1U and T:L2VM1L
1	Channel 2 status	T:L1VAC, T:L1VM2U and T:L1VM2L	T:L2VAC, T:L2VM2U and T:L2VM2L
2	Channel 3 status	T:L1VAC, T:L1VM3U and T:L1VM3L	T:L2VAC, T:L2VM3U and T:L2VM3L
3	Channel 4 status	n/a	T:L2VAC, T:L2VM4U and T:L2VM4L
4	Channel 5 status (spare)	n/a	n/a

Table 9: Type Code 4 - Array of control.

Element Number	Bit Number	Bit Description	ACNET Parameter
0	0	1 = Reset latches for all channels, 0 = do nothing	All ACNET parameters
	1-15	Not used	n/a

Table 10: Channel status bit structure—typical of all channels.

Bit	Bit Description
0	Outside window HI (1 = outside the limit, 0 = within the limit)
1	Outside window LO (1 = outside the limit, 0 = within the limit)
2	1 st to trip (1 = tripped first, 0 = no trip, or not 1 st)
3 - 15	n/a

Vacuum Channel Status Information

The status register bit structure for the CEC protocol is defined in Table 10. A word of status exists for each of the vacuum channels. Good vacuum is defined as being inside an acceptable window, as indicated by the channel's voltage being within an upper and a lower limit.

In principle, when one channel is detected outside a limit, one channel would have gone out of range before the others. Bit 2 of the channel that tripped first will be set.

All status bits values are latched. When they are set to '1' they remain latched until a reset command is issued manually by an operator. Of course, if vacuum is still bad, this condition will be quickly detected and the status will, no doubt, appear to not have reset because of the speed that bad vacuum is detected and latched again.

MECC board design details

The digital board of the interlock circuitry is the Modular Ethernet Configurable Controller (MECC). The MECC board contains a Rabbit Core microprocessor (RCM) and an Altera complex programmable logic device (CPLD). The data acquisition board is connected to the MECC board by way of PCB stackable connectors. The interlock chassis input signals are digitized and the window comparisons are done digitally. Each channel is digitized and comparisons are made at a 5 kHz rate under total control by hardware coded in the CPLD. Digitized vacuum readings and comparison results are stored in CPLD registers upon each acquisition. Trip limit settings are also latched into the CPLD. The response time of the permit signal to bad vacuum condition is, therefore, a maximum of 200 μ s. The RCM is free to obtain vacuum readings, setting values and status at its leisure without affecting the permit signal response time.

Original default trip limit values for the window comparators are listed in Table 13. All trip limit values can be changed at any time and are maintained in flash memory in the RCM. Upon boot up they are reloaded into the CPLD. Table 13 is mainly for a reference if a chassis has been swapped out without having taken note of the trip limit values that were in the chassis that was removed.

The scheduler finite state machine (FSM) that controls data acquisition and window comparisons is described in Table 11. All the CPLD registers are listed in Table 12. The bit structure of the status registers is shown in Table 14.

The Scheduler State Machine

The Scheduler FSM controls the initiation of data acquisition. Once the LTC1867 is started in state Q1, it will wait for the data acquired for each channel to be ready and store it into the appropriate register. The RCM is free to read these registers at any time to obtain vacuum readings.

Table 11: Scheduler FSM.

State	State Clk Length	Tasks	Exit Condition / → Go-to State	Alternate Exit Condition / → Go-to State
Q0	Idle	Wait for 200 μ s timer	ffDAQTimer=1 / →Q1	
Q1	1	Set RunAcq=1 to start data acquisition	None / →Q2	
Q2	Wait	Wait for ADC or time out	DataReady=1 / →Q4	ffDAQTimer=1 / →Q3
Q3	1	Latch error bit (may not be implemented) Reset RunAcq	None / →Q0	
Q4	1	Store vacuum data	None / →Q5	
Q5	1	Latch vacuum comparison result	None / →Q6	
Q6	1	Inc channel counter	None / →Q7	
Q7	1	Decide if done with all the channels	iChanCnt<5 / →Q2	iChanCnt>=5 / →Q8
Q8	1	Reset RunAcq Set iChanCnt = 0	None / →Q0	

CPLD Registers

The CPLD registers are read from and written to by the RCM via the RCM auxiliary I/O bus. Analog values of the vacuum are unipolar from 0 to 10.24 V and are pulled out of the register by the RCM in two bytes as 0x000-0xFFFF binary.

Note, however, that the trip limit values are only one byte wide. Trip limit values are latched into the CPLD by the RCM and comparisons are made on only the most significant byte (MSB) with the acquired vacuum reading. Essentially, the LSB of comparisons are all zero. This gives a resolution on trip limits of 40 mV. The RCM truncates and trip limit setting received by the front end before saving it and writing it to the CPLD.

Table 12: CPLD registers

Rd/Wr	Register	Description	Register Address	Strobe Bit	Strobe Type	Register Data
Rd	Ch1MSB	Channel 1 vacuum	0x6001	PE3	Rd	MSB
Rd	Ch1LSB	Channel 1 vacuum	0x6002	PE3	Rd	LSB
Rd	Ch2MSB	Channel 2 vacuum	0x6003	PE3	Rd	MSB
Rd	Ch2LSB	Channel 2 vacuum	0x6004	PE3	Rd	LSB
Rd	Ch3MSB	Channel 3 vacuum	0x6005	PE3	Rd	MSB
Rd	Ch3LSB	Channel 3 vacuum	0x6006	PE3	Rd	LSB
Rd	Ch4MSB	Channel 4 vacuum	0x6007	PE3	Rd	MSB
Rd	Ch4LSB	Channel 4 vacuum	0x6008	PE3	Rd	LSB
Rd	Ch5MSB	Channel 5 vacuum	0x6009	PE3	Rd	MSB
Rd	Ch5LSB	Channel 5 vacuum	0x600A	PE3	Rd	LSB
Rd	Sts1	Channel 1 status	0x600B	PE3	Rd	value

Rd	Sts2	Channel 2 status	0x600C	PE3	Rd	value
Rd	Sts3	Channel 3 status	0x600D	PE3	Rd	value
Rd	Sts4	Channel 4 status	0x600E	PE3	Rd	value
Rd	Sts5	Channel 5 status	0x600F	PE3	Rd	value
Rd, Wr	Up1	Channel 1 upper limit	0x6010, 0x8010	PE3, PE4	Rd, Wr	value
Rd, Wr	Lo1	Channel 1 lower limit	0x6011, 0x8011	PE3, PE4	Rd, Wr	value
Rd, Wr	Up2	Channel 2 upper limit	0x6012, 0x8012	PE3, PE4	Rd, Wr	value
Rd, Wr	Lo2	Channel 2 lower limit	0x6013, 0x8013	PE3, PE4	Rd, Wr	value
Rd, Wr	Up3	Channel 3 upper limit	0x6014, 0x8014	PE3, PE4	Rd, Wr	value
Rd, Wr	Lo3	Channel 3 lower limit	0x6015, 0x8015	PE3, PE4	Rd, Wr	value
Rd, Wr	Up4	Channel 4 upper limit	0x6016, 0x8016	PE3, PE4	Rd, Wr	value
Rd, Wr	Lo4	Channel 4 lower limit	0x6017, 0x8017	PE3, PE4	Rd, Wr	value
Rd, Wr	Up5	Channel 5 upper limit	0x6018, 0x8018	PE3, PE4	Rd, Wr	value
Rd, Wr	Lo5	Channel 5 lower limit	0x6019, 0x8019	PE3, PE4	Rd, Wr	value
Wr	RstSts	Reset status	0x801A	PE4	Wr	0x01

Table 13: Initial window comparator values

Chassis Channel #	Vacuum Device	Setting Parameter	Voltage Limit	Hex Value
1	T:A0IGTU	T:L2TUU	8.0	0xC800
		T:L2TUL	6.0	0x9600
2	T:A0IPTA	T:L2TAU	8.8	0xDC00
		T:L2TAL	5.8	0x9100
3	T:A0IPTB	T:L2TBU	7.8	0xC300
		T:L2TBL	5.0	0x7D00
4	T:A0IPTD	T:L2TDU	8.8	0xDC00
		T:L2TDL	5.7	0x8E00

Table 14: Channel status bit structure—typical of all channels.

Bit	Bit Description
0	Outside window HI (1 = outside the limit, 0 = within the limit)
1	Outside window LO (1 = outside the limit, 0 = within the limit)
2	1 st to trip (1 = tripped first, 0 = no trip, or not 1 st)
3 - 7	n/a

Reset

There are several reset signals used in the circuitry. The front panel reset resets the trip latches. All the while the button is depressed, the latches are reset and the output permit signal is asserted. If the vacuum is out of range on any channel, however, the permit signal will trip off right away once again when the button is released. This same permit latch reset function is actuated by the remote reset command. This reset signal is quite short, so the permit signal will only be asserted for about 5 μ s if the vacuum is bad when the reset is actuated.

There is a system software reset signal used to reset the CPLD circuitry. This is issued by code in the RCM at power up only. The output line of the RCM used for this is bit 4 on its I/O Port F.