Fermi National Accelerator Lab

Tevatron and Main Injector Sampled Bunch Displays

a.k.a. SBD

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Abstract

This document contains a brief description of the present Sampled Bunch Displays (SBDs) for the Tevatron and Main Injector. It describes the hardware and software at a relatively high level, and provides a description of the longitudinal emittance algorithm. The core of each SBD is a wall-current monitor connected to a 2GHz oscilloscope, the output of which is used to determine longitudinal bunch parameters.

1 Introduction

The Sampled Bunch Display (SBD) is a device for measuring the longitudinal parameters of beam bunches. The raw data consists of the intensity of the passing bunch as a function of time. These parameters may include the intensity, the centroid phase, the RMS bunch length in ns, the emittance in eV·s, and dp/p in units of 10^{-4}. In the Tevatron, the skew and kurtosis of the time distribution is also presented.

2 Physical System

2.1 Hardware

The SBD works by digitizing the output from a wide-bandwidth resistive wall-current monitor (RWCM) [1]. A RWCM consists of a gap in the beampipe wall across which is placed a cylindrically symmetric collection of resistors. As the beam passes these resistors, the image current in the beampipe wall is forced to traverse the resistors producing a voltage which travels along a 7/8" heliax cable to the service building where it is available for use by various front-ends.

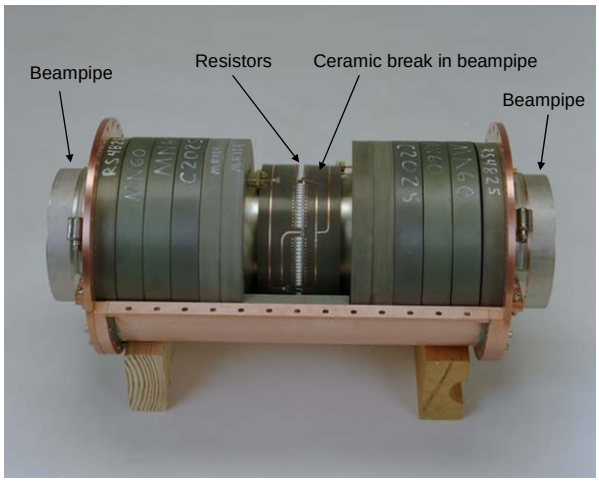

Figure 1: Resistive Wall Current Monitor.

In the service building, the signal for the SBD is split and connected to channels 2 and 3 of a Lecroy Waverunner 6200 oscilloscope running some version of Windows[1]. One of these channels has low gain, while the other has high gain, providing a wider dynamic range than a single 8-bit channel. The scope has a 2 GHz analog bandwidth and digitizes the data at a rate of 5 GHz. After acquisition, the scope data is read by the front-end Power Mac running LabVIEW and processed to obtain the longitudinal bunch parameters. The scope acquisition is controlled by the front-end via a TCP/IP communication link.

[1] The Tevatron scope runs Windows 2000, while the Main Injector scope runs Windows XP.

Table 1: Networked SBD devices and their physical locations.

Hardware	Nodename	Location
MI SBD Computer	SBDMI.FNAL.GOV	Computer Room XGC-108
MI SBD Scope	SBDMISCOPE.FNAL.GOV	MI-60; RR MI60118
TEV SBD Computer	SBDTEV.FNAL.GOV	Computer Room XGC-108
TEV SBD Scope	SBDTEVSCOPE.FNAL.GOV	F0; RR F0107 (bottom)
Hot Spare Computer	INSTEST.FNAL.GOV	Computer Room XGC-108
Hot Spare Scope	SBDSPARESCOPE.FNAL.GOV	F0; RR F0107 (top)
MI Timing Board	MISBDTRIG.FNAL.GOV	MI-60; RR MI60119
MI Timing Spare	MISBDTRIG.FNAL.GOV	MI-60; RR MI60119

2.2 Tevatron Acquisition and Timing

In the Tevatron (TEV), the oscilloscope collects 32 single turn samples and averages them together. The triggers for the scope are generated by a custom NIM module that passes through the proper number of $AA markers which come directly from the RF system. The NIM module settings are controlled by a small LabVIEW executable running on the scope which communicates with the module through the parallel port of the scope. After the requisite number of acquisitions have been accumulated and averaged, the data is transferred from the scope to the front-end LabVIEW program where it is further processed and the cycle repeats. The acquisition cycles happen continuously regardless of whether or not there is beam in the Tevatron.

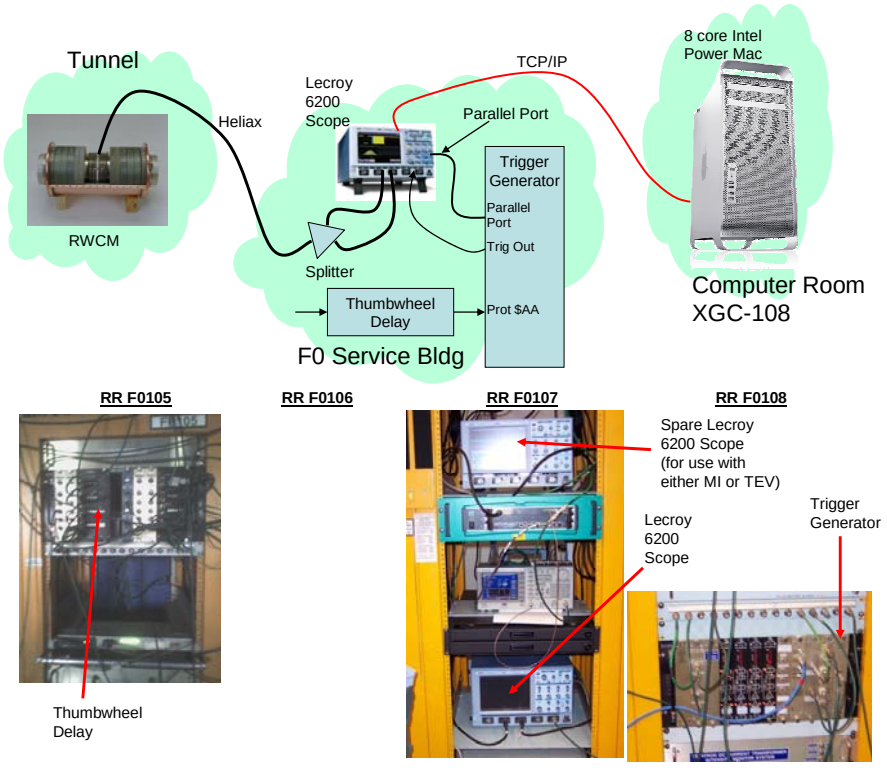

Figure 2: Tevatron SBD system components and connections.

2.3 Main Injector Acquisition and Timing

In the Main Injector (MI), the oscilloscope collects N acquisitions where N depends on the type of MI cycle currently running. Each type of MI cycle has a predefined list of acquisition times referenced to a specified clock event. In addition, some cycles require averaging over a number of samples spaced evenly over the synchrotron period to provide a more reliable emittance measurement. The combination of these two numbers determines how many actual triggers are collected by the scope. The triggers to the scope are generated by a NIM module containing FPGA firmware that listens for 2 clock events specified by the front-end, and then passes through specified $AA markers which arrive directly from the . The specifications are written to the module by the front-end using a telnet connection. The status of the board can be read to determine when the acquisition sequence is finished. At that time, the front-end pushes the data taken by the scope to internal scope memory to await readout by the front-end. This allows the next cycle of triggers to occur while the previous data is being transferred to the front end.