Technical Notes

Digitizer Card Operating Guides

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Document Revision History

Revision Number	Date	Description
1	Jan 4, 2007	Original version

1 Introduction

This is a collection of the several documents previously written.

2 Digitizer Card Mapping in the Control Bus Address Space

The digitizer card can be accessed from the control bus (CB) with 8 data bits and 13 address lines. The upper bits of the address lines are used to distinguish the modules in the crate. Each digitizer card is normally given 256 bytes to be accessed by the controller card.

The information accessible via CB is stored in the digitizer card using block memories and registers implemented in the lower (sums03) FPGA. There are 4 types information accessible via CB: thresholds, operation settings, sums and control registers. The thresholds and operation settings are supported with paging scheme. The data being accessed by the CB and the data being used for module operation can be different. The paging scheme allows users to avoid changing thresholds and operation settings while they are used. The pages being used and being accessed are changed by writing corresponding control registers. The sums are latched as if they are double buffered. However, the sums are actually implemented using similar paging scheme. The users are allowed to take further advantage of the sum implementation.

The particular addresses of the contents can be assigned in two different mappings: the original mapping and native mapping. The contents stored in the digitizer cards internally using native mapping. The contents are remapped via an address translation ROM to the original mapping so that originally written test software can still be used. The contents normally to be readout together are organized together in the native mapping. The users are allowed to take advantage of native mapping to write faster and simpler software. The switching between the mappings is purely software operation; simply set or reset the bit 7 of the FF register (at address 0xFF). The power on default is the original mapping.

The digitizer card also supports both individual and broadcast accesses. Each digitizer card in the crate can be accessed individually at the assigned card address. All the cards in the crate can be written simultaneously at the broadcast address. The broadcast ability allows the cards to change operation state (such as threshold page to be used) together.

2.1 The Native Mapping

The native mapping of the digitizer card is shown in the following table. The digitizer presents the native mapping when the bit 7 of the FF register is set (=1xxxxxxx_b).

00		R/W	Threshold	Immediate	ch	0
04						1
08						2
0C						3
10		R/W		Fast	ch	0
14						1
18						2
1C						3
20		R/W		Slow	ch	0
24						1
28						2
2C						3
30		R/W		Very Slow	ch	0
34						1
38						2
3C						3
40		R/W	Sum Length	Immediate		
42		R/W		Fast		
44		R/W		Slow		
46		R/W		Very Slow		
48		R/W	Constant		ch	0
4A						1
4C						2
4E						3
50		R/W	Squlch Level		ch	0
52						1
54						2
56						3
58		R/W	Pedestal_LO		ch	0
5A						1
5C						2
5E						3
60		R/W	Pedestal_HI		ch	0
62						1
64						2
66						3
68		R/W	Mode Select		ch	0
6A						1
6C						2
6E						3
70		R/W	DAC Out		ch	0
72						1
74						2
76						3
78		R/W	Test DAC			
7A		R/W	MaxDY	=0x80		
7C		R/W	CIC Length	=124-128		
7E		R/W	Ped Length	=750-752		
80		R	Sum	De-rippled	ch	0
84						1
88						2
8C						3
90		R		Fast	ch	0
94						1
98						2
9C						3
A0		R		Slow	ch	0
A4						1
A8						2
AC						3
B0		R		Very Slow	ch	0
B4						1
B8						2
BC						3
C0		R	INTEG/CIC_WF		ch	0
C8						1
D0						2
D8						3
E0		R/W	THR U page			
E1		R/W	THR C page			
E2		R/W	Constant U page			
E3		R/W	Constant C page			
E4		R/W	Sum U page			
E5		R/W	Sum F page			
E6		R/W	Sum S page			
E7		R/W	Sum V page			
F6		R	Circular Buffer PT			
F8		R/W	FPGA Ctrl Reg.			
FC		R	Temperature			
FF		R/W	FF reg			

The thresholds from address 0x00 to 0x3F are 32-bit numbers each occupying 4 bytes. The LSB of the threshold has a lower address. There are 64 pages of thresholds. The pages being used and being accessed via CB are represented by the lower 6 bits of the "THR U page" (at 0xE0) and the "THR C page" (at 0xE1) registers, respectively.

The addresses from 0x40 to 0x7F contain the settings for the module operation. There are 8 pages for this class of information. The pages being used and being accessed via CB are represented by the lower 3 bits of the "Constant U page" (at 0xE2) and the "Constant C page" (at 0xE3) registers, respectively.

The addresses from 0x80 to 0xDF are assigned for sums. The fast, slow and very slow sliding sums are 32-bit integers taking 4 bytes each. The LSB has lower address. The immediate measurements are implemented as sliding sums with sum length =1. On power on, the sum length (at 0x40 and 0x41) for immediate is automatically preset to 1, i.e., (0x40) = 0x01 and (0x41) = 0x00. The users need not to set the sum length for immediate for regular operation. However, the immediate sums are stored internally and not output. The de-rippled sums are output at addresses 0x80 to 0x8F, 4 bytes for each channel. The de-rippled sums are not used to compare with thresholds. They are primarily for display only. The integrations are 64-bit integers and are readout from 0xC0 to 0xDF in normal operation. Two other useful numbers the waveform WF and the CIC sums can be readout form the same location if the bit 4 of FF register is set =1. The CIC sum is a sliding sum of sliding sum. It filters out higher frequency noise better than sliding sum. The waveform is stored in the internal memory and is used in de-ripple process.

There are 8 pages for the sums. The pages being used and being accessed via CB are represented by the lower 3 bits of the "Sum U page" (at 0xE4), the "Sum F page" (at 0xE5), the "Sum S page" (at 0xE6) and the "Sum V page" (at 0xE7) registers, respectively. All the page registers are reset on power up and can be read and written by the Controller Card. When the latch sum signals for fast, slow and/or very slow become active, the sum F, S and/or V pages are updated to the current value of the Sum U page and then the Sum U page increases by 1. So the corresponding pages for different sum types point to the last latched values unless more than 8 latch commands have been issued before the sums are readout. The bit 7 of the sum F, S and V page registers are used to prevent the registers from being updated by the latch sum signals. The user may set the bit 7 of the page registers before reading the sums so that the contents are not corrupted by the new latch sum signals.

The contents of de-rippled sums and the integrations are pointed by the Sum F page and the Sum V page registers, respectively.

2.2 The Original Mapping

The original mapping is shown in the following table. The digitizer presents the original mapping when the bit 7 of the FF register is reset (=0xxxxxxx_b). The original mapping is also the power on default condition.

00		R/W	Threshold	Fast	ch	0
04		R/W		Slow	ch	0
08		R/W		Very Slow	ch	0
0C		R/W		Immediate	ch	0
10		R	Sum	Fast	ch	0
14		R		Slow	ch	0
18		R		Very Slow	ch	0
1C		R/W	Mode Select		ch	0
1E		R/W	DAC Out		ch	0
20		R	Sum	De-rippled	ch	0
22		R/W	Pedestal_HI		ch	0
24		R/W	Constant		ch	0
26		R/W	Pedestal_LO		ch	0
28		R	INTEG/CIC_WF		ch	0
30		R/W	Threshold	Fast	ch	1
34		R/W		Slow	ch	1
38		R/W		Very Slow	ch	1
3C		R/W		Immediate	ch	1
40		R	Sum	Fast	ch	1
44		R		Slow	ch	1
48		R		Very Slow	ch	1
4C		R/W	Mode Select		ch	1
4E		R/W	DAC Out		ch	1
50		R	Sum	De-rippled	ch	1
52		R/W	Pedestal_HI		ch	1
54		R/W	Constant		ch	1
56		R/W	Pedestal_LO		ch	1
58		R	INTEG/CIC_WF		ch	1
60		R/W	Threshold	Fast	ch	2
64		R/W		Slow	ch	2
68		R/W		Very Slow	ch	2
6C		R/W		Immediate	ch	2
70		R	Sum	Fast	ch	2
74		R		Slow	ch	2
78		R		Very Slow	ch	2
7C		R/W	Mode Select		ch	2
7E		R/W	DAC Out		ch	2
80		R	Sum	De-rippled	ch	2
82		R/W	Pedestal_HI		ch	2
84		R/W	Constant		ch	2
86		R/W	Pedestal_LO		ch	2
88		R	INTEG/CIC_WF		ch	2
90		R/W	Threshold	Fast	ch	3
94		R/W		Slow	ch	3
98		R/W		Very Slow	ch	3
9C		R/W		Immediate	ch	3
A0		R	Sum	Fast	ch	3
A4		R		Slow	ch	3
A8		R		Very Slow	ch	3
AC		R/W	Mode Select		ch	3
AE		R/W	DAC Out		ch	3
B0		R	Sum	De-rippled	ch	3
B2		R/W	Pedestal_HI		ch	3
B4		R/W	Constant		ch	3
B6		R/W	Pedestal_LO		ch	3
B8		R	INTEG/CIC_WF		ch	3
C0		R	Sum	Immediate	ch	0
C4						1
C8						2
CC						3
D0		R/W	Squlch Level		ch	0
D2						1
D4						2
D6						3
DA		R/W	MaxDY	=62		
DC		R/W	CIC Length	=124-128		
E0		R/W	THR U page			
E1		R/W	THR C page			
E2		R/W	Constant U page			
E3		R/W	Constant C page			
E4		R/W	Sum U page			
E5		R/W	Sum F page			
E6		R/W	Sum S page			
E7		R/W	Sum V page			
EA		R/W	Ped Length	=750-752		
EC		R/W	Sum Length	Immediate		
F0		R/W		Fast		
F2		R/W		Slow		
F4		R/W		Very Slow		
F6		R	Circular Buffer PT			
F8		R/W	FPGA Ctrl Reg.			
FA		R/W	Test DAC			
FC		R	Temperature			
FF		R/W	FF reg			

The contents are kept at the original locations in the original mapping. The newly added contents are added to the originally unused space. The de-rippled sums at 0x20, 0x50, 0x80 and 0xB0 are 16-bit integers as originally defined. The 32-bit version of the de-rippled sums is mapped from C0 to CF. The sum length for immediate is stored at 0xEC which is preset to =1 at power on.

2.3 The Broadcast Access

The CB address space has 13 bits. The digitizer card individual access address is 0x0NXX, where N = 0 to E is the board switch setting and XX = 00 to FF is the byte address.

The digitizer card broadcast access use the address space outside the above. The address is 0x13XX which was unused by any card. In the broadcast access address space, all digitizer cards are selected as being individually accessed.

- Writing to a location in 0x13XX causes the addressed byte in all cards being written with the same value.
- Reading in the 0x13XX space is not recommended since the bus conflict may be resulted in. Reading-after-writing is allowed since the anticipated values from all cards are identical but may not be very useful.

The broadcast access is essentially used to change operating condition of all cards simultaneously. For example, one may change the threshold page being used when a machine state change is needed.

3 The Integration Operation

The digitizer card computes sliding sums and integrations triggered by the MAKE_MEAS signal. In typical operation, the signal is generated by the TC about every 21 μs. The integrations are 64-bit long integers readable from the control bus at 8 bytes each.

The integration process begins after the sums are reset. The first set of measurement points can be ignored and the number of points to be ignored is defined by users. Then the pedestals of the 4 channels are accumulated. The pedestals are stored once the accumulation is done.

Meanwhile, sliding sums are kept. In the integration mode, very slow sliding sum for each channel is used as input data participating the squelch checking and the integration accumulation.

After the pedestals become available, the very slow sliding sums are used to compare with the pedestals plus the squelch levels to see if valid data present or not. If the very slow sum of a channel is higher than the pedestal plus the squelch level, the pedestals is subtracted from the very slow sum and the result is accumulated to the integration.

A sufficiently large initial value is given to the integrations. The initial value prevents the integrations from drifting to negative, when the pedestals are calculated to be too high.

In the integration mode, pre-defined 32-bits from the 64-bit integration are compared with the 32-bit very slow thresholds every 21 μs. The details are described below.

The users can control the integration operation by setting several parameters accessible from the control bus.

3.1 The Parameters Relevant to the Integration Mode

The native mapping will be used in this section. The digitizer presents the native mapping when the bit 7 of the FF register is set (=1xxxxxxx_b). For the original mapping of the digitizer card when the bit 7 of the FF register is clear (=0xxxxxxx_b), see the last section.

The following parameters and registers are to be used in order to control the integration operation:

- The FF register.

- The FPGA Control register.
- The Mode Select registers.
- The Sum Lengths.
- The Pedestals
- The Thresholds

3.1.1 The FF Register

The FF register is always at address 0xFF in both native and original mapping. The bit 7 of the FF register is used to control the mapping for the control bus. In this document, native mapping is used, which requires the bit 7 being set. To use the original mapping, bit 7 is clear.

Bit 7	6	5	4	3	2	1	0
Mapping	Ch OK		Out De-Bug		Do Sums	Clear Sums	

The bit 1 and 2 are used to initialize sum operations without timing card. Turning the bit 1 high and then low causes the digitizer card to initialize the summing operation. Turning the bit 2 high and then low causes the digitizer card to accumulate sliding sums and integrations.

The summing operation via toggling the FF register bit 1 and 2 is usually for debugging purposes and the input data are always the constants stored in addresses 0x48 to 0x4F. The bit 0 in the FPGA Control Register should be set in order to use constant as the summing and integration input.

3.1.2 The FPGA Control Register

The FPGA Control Register is a 16-bit register at address 0xF8 and 0xF9 in both native and original mapping. At current time, only the following bits are used:

Bit15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSKIP16								DK[7..1]							Use constant

When bit 0 is set, constants loaded at 0x48 to 0x4F (in native mapping) are used as input values for computing sliding sums and integrations. In normal operation using real ADC input, the bit 0 is clear. The bit 8 to bit 15 represents a number NSKIP16 that are loaded by the users. The digitizer card ignores the first 16*NSKIP16 measurements before starting summing and integration processes. The bit field DK[7..1] is used to specify offset for the decimation constant for the de-ripple process.

3.1.3 The Mode Select Registers

The Mode Select Registers are 16-bit words at 0x68 to 0x6F (in native mapping). Each channel is controlled by its own Mode Select Register. The bits of the registers are assigned as shown in the following table:

Bit15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							Squelch	INP_ON/	MADC Function Select [2:0]			Use Integration Mode	Test Mode On	Enable Long Time Constant	Enable High Range

Most bits in the Mode Select Registers are defined in “BLM Upgrade Users Guide”. Only bit 3 and bit 8 will be described here.

When bit 3, “Use Integration Mode” is turned on, the 32-bit very slow thresholds will be compared with the bits 16 to 48 of the integrations. When the “Use Integration Mode” bit is clear, the integrations will still be accumulated, but they are not compared with the thresholds.

Setting bit 8 “Squelch” high will turn on the squelch operation. Inputs lower than the sum of the pedestal plus squelch level are considered noise and are not accumulated into the integration.

3.1.4 The Sum Lengths

The lengths of the sliding sums are 16-bit integers. In addition to the fast, slow and very slow sliding sums, the immediate measurement for each channel is also implemented as a sliding sum with length =1. All these sums are implemented identically and their lengths can be arbitrarily defined by the users.

The pedestal sum length at 0x7E is defined similarly. The length is used to calculate the pedestals at the beginning of the run. In the integration mode, very slow sliding sum is used as the input. We currently defined a fix ratio between the very slow sum length and the pedestal sum length. The pedestal sum length must be 16 times of the very slow sum length. Typically, the very slow sum length is chosen to be about 47 and the pedestal length to be about 752.

Note that the users are allowed to choose very slow sum length freely. For example, the very slow sum length can be 55 and the pedestal sum length 880.

3.1.5 The Pedestals

The pedestals are accumulated automatically at the start of a run. As mentioned earlier, the first 16*NSKIP16 measurements are ignored before the pedestals are calculated. Accumulating the pedestals uses number of measurements that equals to the pedestal length.

The calculated pedestals are placed into the RAM block interfacing with the control bus. The users are allowed to read the pedestals out. The pedestals can be changed by the users also, if necessary. But to avoid being overwritten, it can only be changed after the accumulation of the pedestals at the beginning of each run. A clean way to change pedestal is to use page changing via broadcast. See “Digitizer Card Mapping in the Control Bus Address Space” for detail..

3.1.6 The Thresholds

When bit 3 of the Mode Select Registers, “Use Integration Mode” is turned on, the 32-bit very slow thresholds will be compared with the bits 16 to 47 of the integrations. When the “Use Integration Mode” bit is clear, the very slow sliding sums are compared with the very slow thresholds.

Pre-loaded set of thresholds are organized as pages and there are 64 pages total in a digitizer card. The users are allowed to select a particular page to be used at any time. A clean way to change page is via broadcast. See “Digitizer Card Mapping in the Control Bus Address Space” for detail.

3.2 The Equations

We try to write down the equations of the variables mentioned above. Define:

N_S = the NSKIP16 parameter.

L_{PED} = the pedestal sum length.

L_{VS} = the very slow sum length.

X_i = the raw measurement data.

S_i = the very slow sliding sum.

P = the pedestal.

q = the squelch level.

Y_i = the integration.

First, the pedestal is actually a sum of the first set of measurements.

$$P = \sum_{i=16N_S}^{(16N_s+L_{PED}-1)} X_i$$

The very slow sliding sum can be viewed as an average of a set of measurements.

$$S_j = \sum_{i=L_{VS}-j+1}^{j} X_i$$

The integration is the integration of the averaged inputs, i.e., the very slow sliding sums.

$$Y_k = (128 \times 1024 \times 1024) + \sum_{j=(16N_s+L_{PED})}^{k} (16S_j - P)u(16S_j - P - q)$$

An initial value of 128M is given to the integration so that it will not drift to negative. The step function u(x) is defined =0 when x<0 and =1 when x>0.

3.3 Bit Alignment

As can be see above, divisions are not actually taken when the variables are to be interpreted as averages such as pedestals and very slow sliding sums. The values are scaled according the corresponding sum lengths.

In the FPGA implementation the variables are aligned based on the following picture:

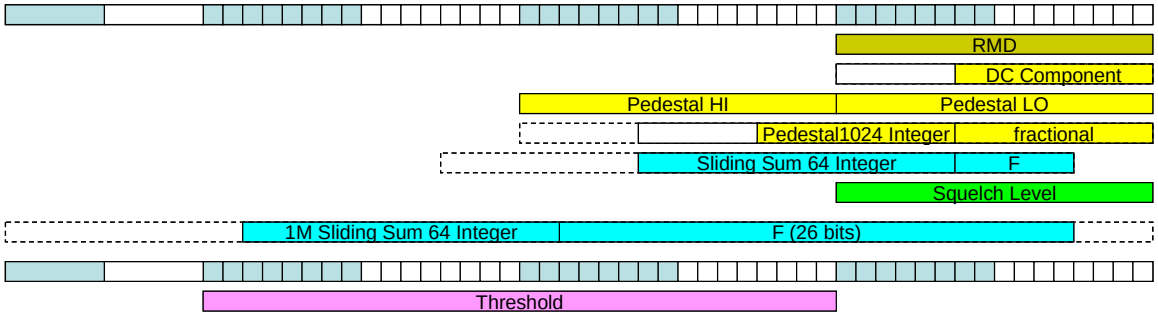

Figure 3.1
Bit Alignment for Integration Operation

The pedestals and sliding sums are accumulated aligned with the raw measurement data. The squelch level is added to the pedestal with bit 0 aligned. Therefore, it is possible set squelch level with fractional part.

When the very slow sliding sums are operated with pedestals and squelch levels, the sliding sums are shifted up for 4 bits equivalent to multiplying by 16.

The integration is aligned with the pedestals. Therefore, dividing the integration value by L_{PED} scales it back to the raw measurement data unit.

The thresholds are aligned to the bit 16 to 47 of the integration.

4 The De-rippled Process

The signal cables in the MI tunnel pick up noise generated by equipments powered by 3-phase 60Hz AC. It contains primarily harmonies of 60Hz, 180Hz and multiples of 360Hz. The noise level is higher than desired signal and the noise peaks exist at both higher and lower frequencies comparing with the signal spectrum. A typical set of raw measurement data and their spectrum are shown in Figure 4.1.

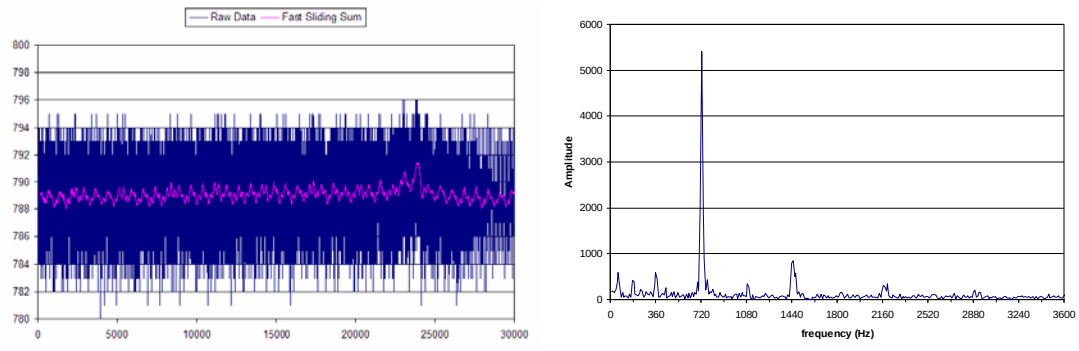

Figure 4.1
Raw Measurement Data and Their Spectrum

Calculating sliding sums can be viewed as a digital filtering process. The fast sliding sum over length of 128 shown in Figure 4.1 has reduced noise level from about 10 ADC counts in raw data down to about 2 ADC counts. Some beam loss can be seen from fast sliding sum plot.

However, the sliding sum is a low pass filter with sinc(f) function shaped frequency responds. The zeros of the sinc(f) is very sharp and it is hard to align with noise peaks, especially when the sampling frequency is not integer multiple of 60Hz and when accelerator ramps which varies the sampling frequency. Also the side lobe of the sinc(f) is not low enough. Therefore, the plot of fast sliding sum still contains glitches along with unfiltered 60Hz and 180Hz components.

The de-ripple process further eliminates remaining noise components so that smaller beam losses become visible. The process takes following several steps:

1. Calculating the Cascade Integration-Comb (CIC) sums.
2. Waveform extraction, storage and validation.
3. Waveform subtraction.

4.1 Calculating the Cascade Integration-Comb (CIC) Sums

The cascade integration-comb (CIC) digital filter of order N contains N cascaded stages. Each stage is a moving average filter which is a CIC filter of order 1. Sliding sum can be viewed as a CIC filter of order 1 with un-normalized gain. The CIC sums implemented in the sum03 FPGA firmware is the CIC filter of order 2, which is the sliding sum of the sliding sum.

The frequency responds shape of the CIC sums is $\text{sinc}^2(f)$ in which the zeros become the second order ones that provide deeper attenuation to the noise peaks even the peaks are not precisely aligned with the zeros. The side lobes become lower. In Figure 4.2, the sliding sums and the CIC sums of a set of typical measurement data are plotted (with appropriate scales and an artificial offset). It can be seen that the CIC sums are significantly smoother.

The sum length K for the CIC sums is chosen to be 124-128, which brings the first zero to 360Hz. It can be reasonably assume that the CIC sums are band limited to 360Hz.

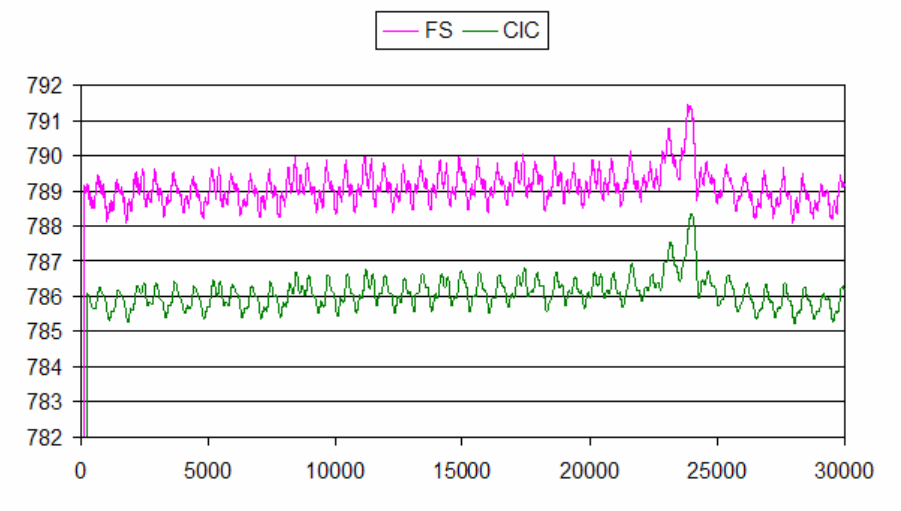

Figure 4.2
Fast Sliding Sums and the CIC Sums

The CIC sum $y[n]$ and sliding sum $s[m]$ of input sequence $x[j]$ with sum length K in our work are defined as:

$$y[n] = \sum_{m=n}^{n-(K-1)} s[m] \quad s[m] = \sum_{j=m}^{m-(K-1)} x[j]$$

In the practical firmware, the accumulations above are implemented recursively as shown in Figure 4.3.

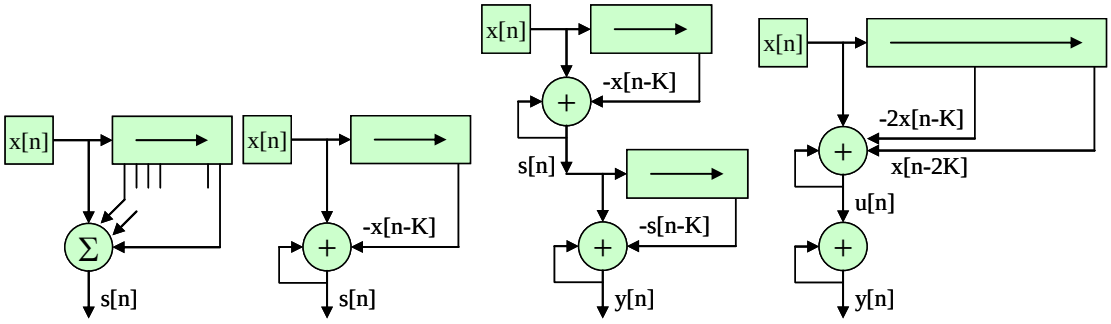

Figure 4.3
Computation of the Sliding Sums and the CIC Sums

For example, instead adding K times as shown in the first diagram in Figure 4.3 for each data point, the sliding sum is actually calculated as shown in second diagram with one addition and one subtraction:

$$s[m] = s[m-1] + x[m] - x[m-K] \quad s[j] = 0,\ x[j] = 0 : j < 0$$

While calculating CIC sum $y[n]$, we would like avoid adding a separate storage for $s[m]$, given that a record of up to 64K raw measurement points $x[j]$ are available. Instead of using the third diagram in Figure 4.3 to calculate the CIC sum, the formula is altered as show in the right most diagram which contains two recursive accumulations:

$$u[n] = u[n-1] + x[n] - 2x[n-K] + x[n-2K]$$

$$y[n] = y[n-1] + u[n]$$

This way, the only additional storage is the intermediate value $u[n]$ which takes one memory space and no additional long record of intermediate values is to be stored.

4.2 Waveform Extraction, Storage and Validation

In the BLM digitizer FPGA firmware, the calculated CIC sums are directly stored as the waveform data. Since the CIC sums are band limited to about 360Hz, it is possible to decimate the y[n] sequence to save storage space without losing data. The decimation counter is a 24-bit accumulator that increases by the decimation constant DM (=22336 for MI) for every input point or about every 21-22 μs. The top 7 bits are used as address to the waveform WF storage memories. This way, 128 CIC sum points are stored for the time period corresponding to 60Hz. The separation of two points is 5 or 6. The effects of non-uniform decimation are negligible for our application, although interpolation algorithms are available to reduce the effects. The block diagram of the de-ripple processor is shown in Figure 4.4.

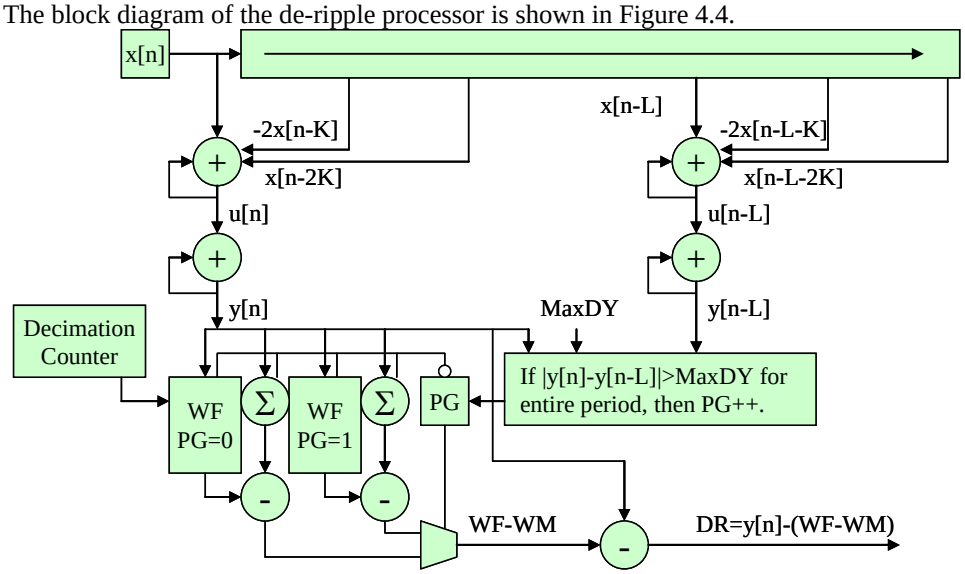

Figure 4.4
The De-ripple Processor

The waveform storage memories are split into two pages for each channel. The CIC sums are written into the page as the tentative waveform which must be validated through the period. Meanwhile, for each channel, a sum of the waveform is accumulated to calculate the waveform mean WM value. After accumulating 128 points for the entire period, the sum is simply the waveform mean scaled by factor of 128, or 7 bits. This is the reason of choosing the decimation scheme mentioned above.

Two CIC sums are calculated, the current one y[n] and the one a period before y[n-L], where L is the length corresponding to a period which is about 752. During the period, the absolute value of the difference of the two CIC sums is constantly checked with a parameter MaxDY. If the difference between the two CIC sums is too big, there may be an abrupt beam loss in the period. The waveform then is considered invalid. If the differences in the entire period are within the predefined limit, the waveform becomes valid.

At the end of each period, if the waveform is valid, a 1-bit counter PG flips, which swap the tentative waveform page to the usable waveform page. The new tentative waveform is stored in another page until it becomes valid waveform at the end of another period.

At the initial time after reset, the firmware logic forces the value (WF-WM)=0. After the waveform of a period become valid, it always outputs the latest valid one.

4.3 Waveform Subtraction

Once the waveform become valid, waveform subtraction can be performed to get the de-rippled sum DR. The stored waveform WF contains DC component which represents the slow beam loss at the period when the waveform is recorded. To assure the slow beam loss at current time is corrected preserved, the DC balanced waveform (WF-WM) is used in the subtraction. As mentioned above, the WM is the waveform

mean accumulated during the waveform recording period. The full de-ripple process is shown in Figure 4.5.

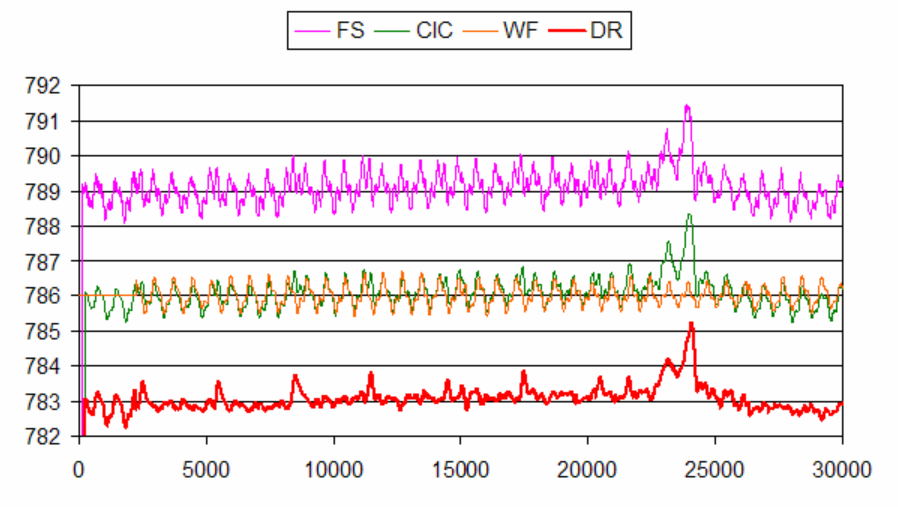

Figure 4.5
The De-ripple Process

In order to see the curves clearly, each curve are added with an offset. (Or they will all overlap on each other.) The second curve is the CIC sum with sum length of 128. For reference, the sliding sum FS with same sum length is also shown. The waveform WF in general takes 3 periods to become valid. In the first 3 periods, WF and WM are forces to be 0. The de-rippled outputs DR first follow the CIC sum for 3 periods since WF is invalid. Then it becomes a smooth curve with 60Hz and 180Hz ripples canceled. Both abrupt and slow beam losses of become visible.

4.4 Operation Guide

The de-rippled sums can be readout as regular sliding sums. The following is a check list for appropriate settings. (All addresses are in the Native Mapping.)

1. In MI, set CIC length at 0x7C 124 (=(1/360Hz)/22.18μs) to 128.
2. In MI, set pedestal length at 0x7E 752 (=(1/60Hz)/22.18μs). If in calculating integration, the very slow sum length at 0x46 must be 1/16 of pedestal length which should 47.
3. In Tevtron, set CIC length around 132 (=(1/360Hz)/21μs), set the pedestal length 794 (=(1/60Hz)/21μs) and set the decimation constant DM 21152 (=16M/((1/60Hz)/21μs)). In order to change DM, bit field DK[7..1] at 0xF8 is set. Note that 0xF8 is the FPGA control register. Make sure bit 0 ("Use Constant") is 0 while using real ADC data. DM = 22336 +/- 32*DK[6..1], where +/- is determined by DK[7]=0/1. So let DK[7..1]=1100 101 will set DM = 21152.
4. For MI operation, DK[7..0]=0 will set DM = 22336, the user may fine tune this value by setting DK[7..1] as described above.
5. Set MaxDY at 0x7A 0x80, which represents a scaling of 0.5 ADC count if CIC sum length is 128.
6. The de-rippled sum can be readout from 0x80 to 0x8F, 4 bytes per channel. The scaling factor is the CIC length squared, i.e., 124x124 to 128x128.
7. If the bit 4 of FF Register, Out De-Bug is set, two additional numbers for each channel are output from 0xC0 to DF. The waveform WF for channels 0 to 3 are output from 0xC0, 0xC8, 0xD0 and 0xD8, respectively. The CIC sums are output from 0xC4, 0xCC, 0xD4 and 0xDC, respectively. They all have the same scale. The WF has an offset of 0x1000000. It is DC balanced around this offset.

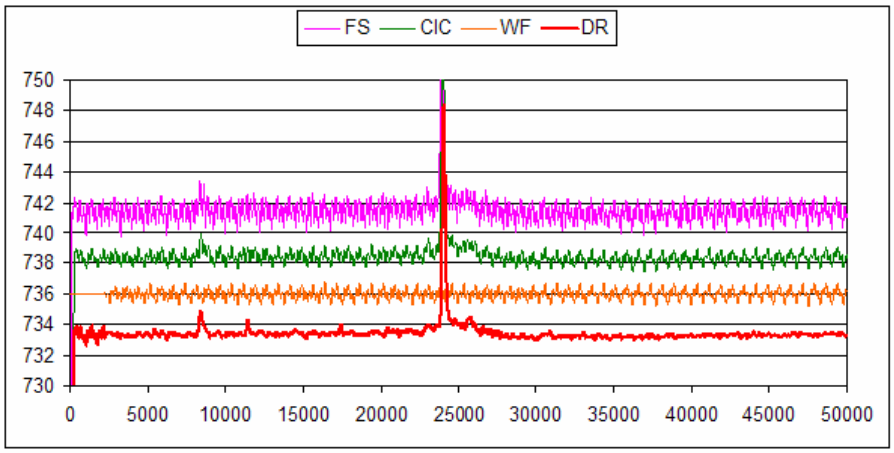

Figure 4.6
The De-ripple Process for LM322

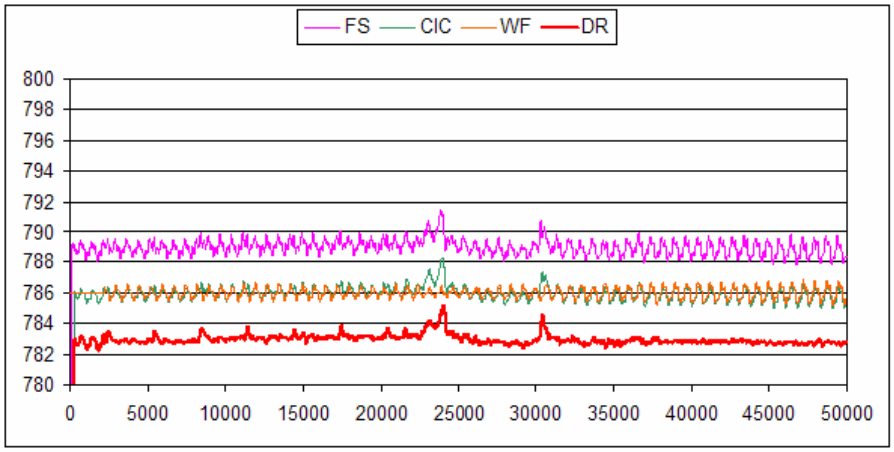

Figure 4.7
The De-ripple Process for LM402c

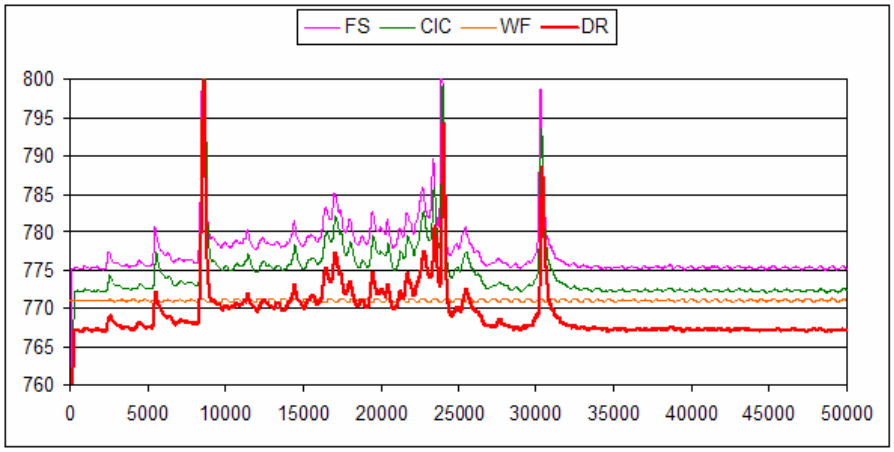

Figure 4.8
The De-ripple Process for LM608a