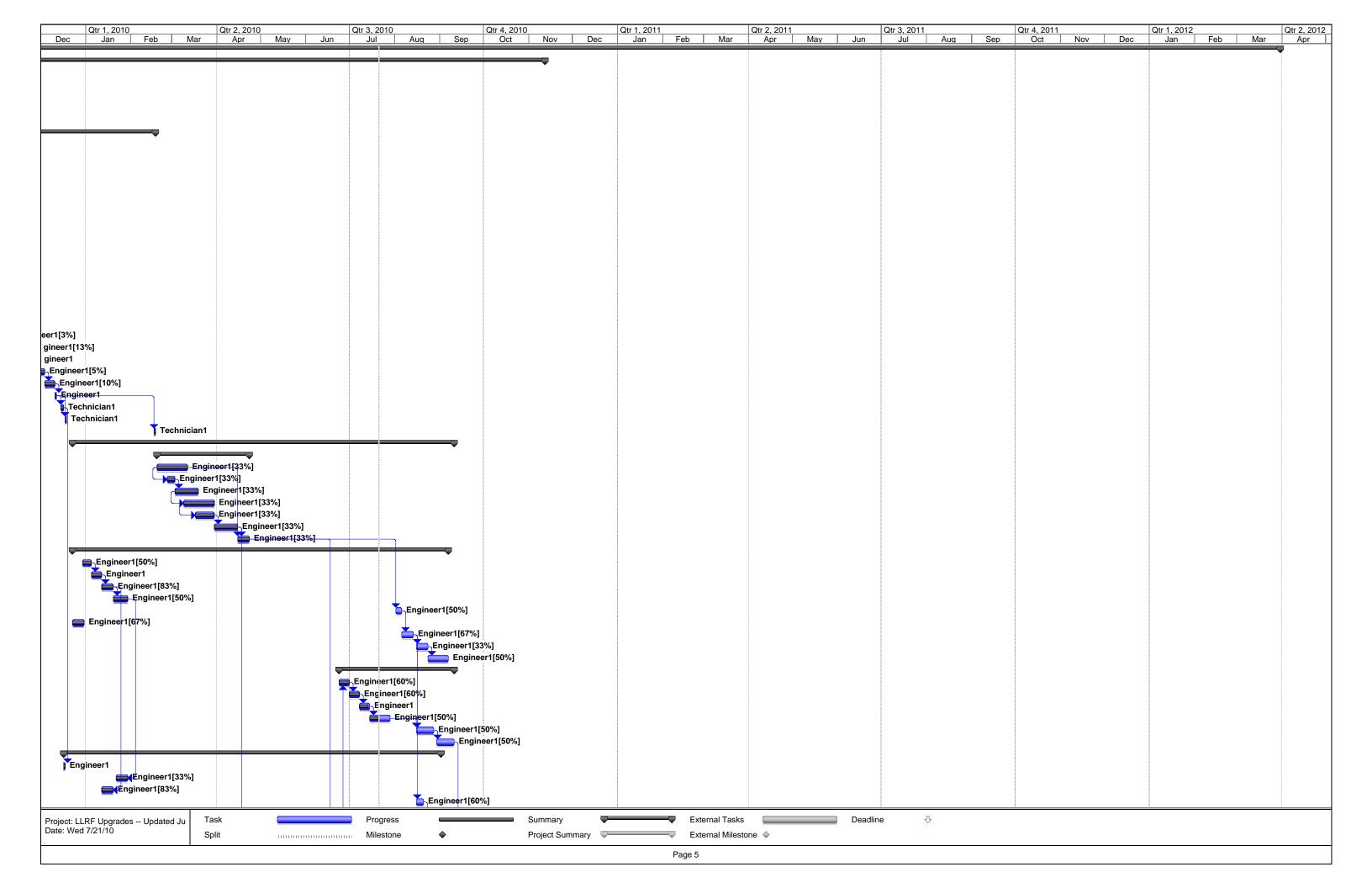
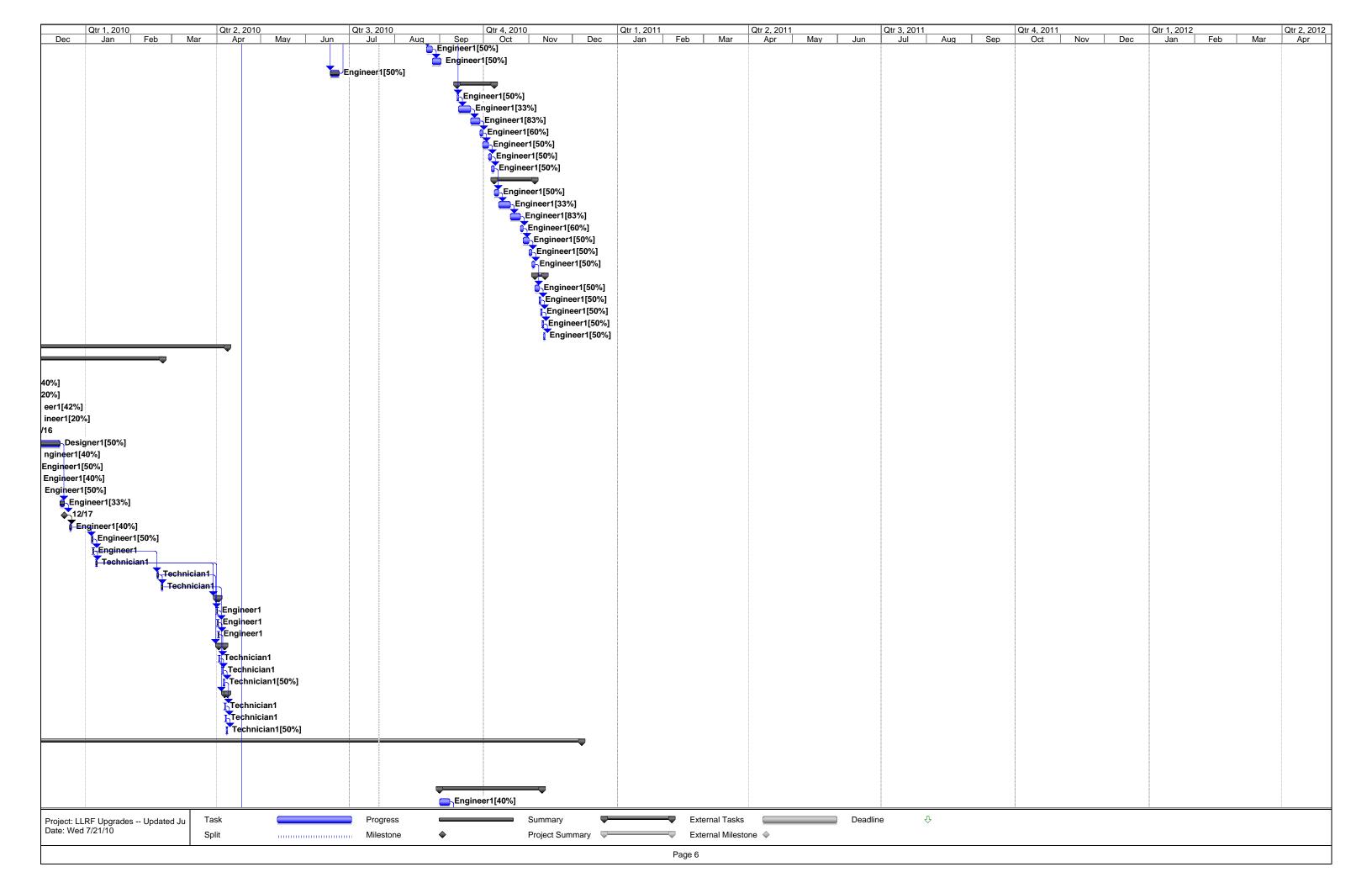
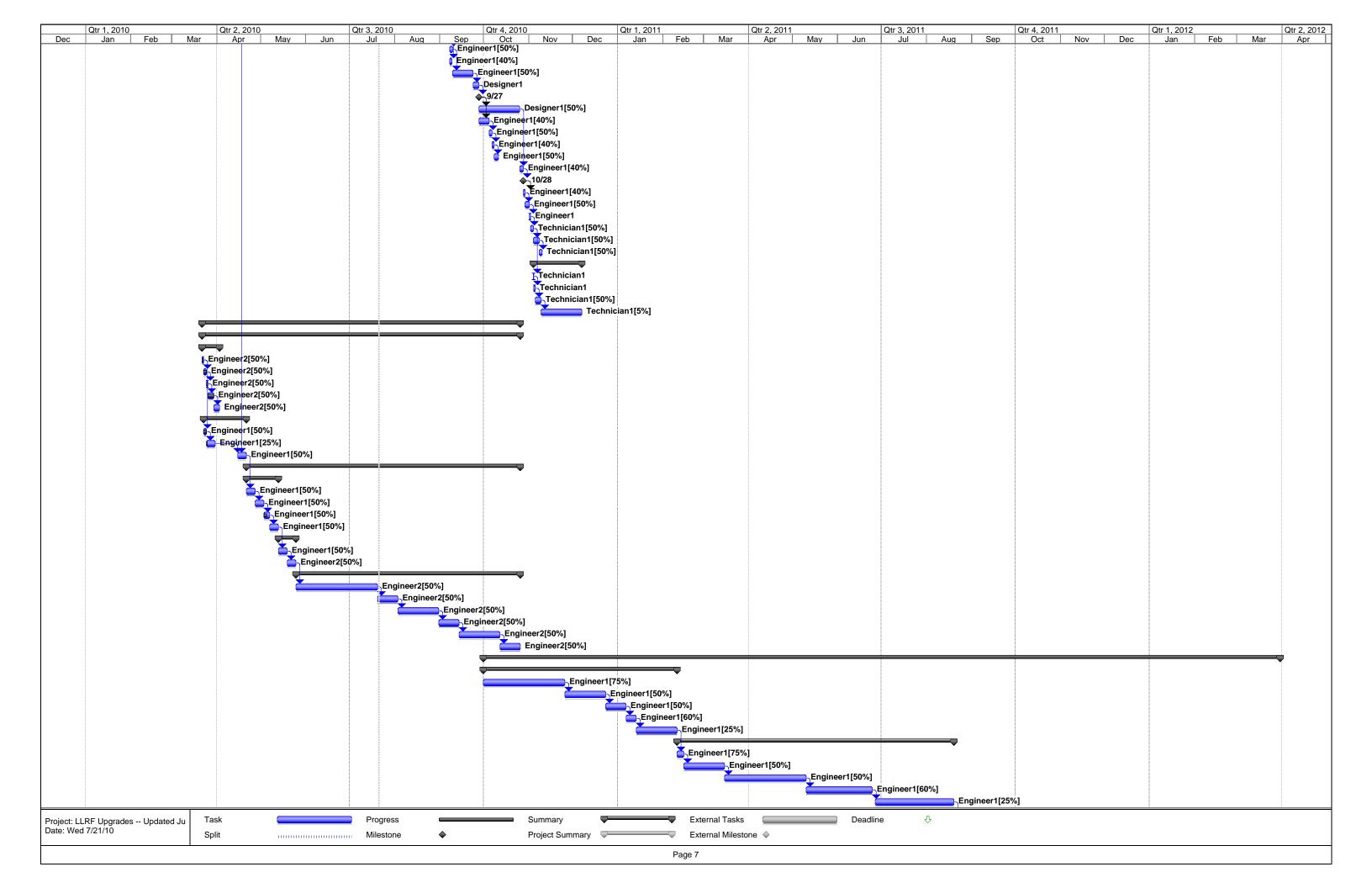
Task	Name	Start	Finish Predecessors	Duration	Work	% Complete Qtr 4, 2008 Oct	Qtr 1, 2009 Nov Dec Jan Feb Mar	Qtr 2, 2009 Qtr 3, 2009 Apr May Jun Jul Aug Sep	Oct Nov
_	F Electronics Upgrades	Wed 11/19/08	Fri 3/30/12	878 days	4,319.2 hrs	45%	V Total		
	DDS_01: LLRF Frequency and Phase Control	Wed 11/19/08	Fri 11/12/10	517.09 days	1,843.2 hrs	82%	-		
	DDS Component Evaluation Testing	Wed 11/19/08	Wed 2/4/09	56 days	328 hrs	100%	▽		
	Evaluation Modules Procured	Wed 11/19/08	Wed 11/19/08	1 day	8 hrs	100%	Engineer1		
_	Hardware Integration	Thu 11/20/08	Wed 1/7/09 4	35 days	160 hrs	100%	Engineer1[57%]		
	FPGA Code Development	Thu 1/8/09	Wed 2/4/09 5	20 days	120 hrs	100%	Engineer1[75%]		
_	Testing	Thu 1/22/09	Wed 2/4/09 6SS+10 days	10 days	40 hrs	100%	Engineer1[50%]		
	DDS VME Prototype Hardware Development Prototype Design Begins	Mon 2/9/09	Wed 2/17/10 Mon 2/9/09	268 days	527.2 hrs 0 hrs	100% 100%	A 2/0		
	Initial Design and Layout	Mon 2/9/09 Mon 2/9/09	Fri 3/6/09 9	0 days 20 days	160 hrs	100%	♦ <u>2/9</u>	ineer1	
	PCB Parts and Symbol Development	Mon 3/2/09	Fri 5/22/09 0SS+15 days	60 days	16 hrs	100%	Liigi	Designer1[3%]	
-	Schematic Capture and Board Layout	Mon 3/9/09	Fri 5/1/09 10	40 days	160 hrs	100%		Engineer1[50%]	
_	PCB Layout Specification	Mon 5/4/09	Fri 5/15/09 12	10 days	16 hrs	100%		Engineer [20%]	
	PCB Layout Begins	Tue 6/9/09	Tue 6/9/09 13	0 days	0 hrs	100%		6/9	
	PCB Layout	Tue 6/9/09	Mon 9/28/09 14	80 days	19.2 hrs	100%			Designer1[3%]
	PCB Design Complete	Mon 9/28/09	Mon 9/28/09 15	0 days	0 hrs	100%			9/28
	Build BOM and Assembly Parts Database	Mon 5/25/09	Wed 6/10/09 11	13 days	40 hrs	100%		Engineer1[38%]	
	Sample Components Ordered	Thu 6/11/09	Thu 6/11/09 17	1 day	4 hrs	100%		Engineer1[50%]	
_	Sample Components Delivered	Fri 6/12/09	Thu 6/25/09 18	10 days	4 hrs	100%		Engineer1[5%]	
	Protoype Component Orders Compiled	Fri 6/26/09	Thu 7/2/09 19	5 days	8 hrs	100%		Engineer1[20%]	
	Protoype Components Ordered	Tue 7/7/09	Tue 7/7/09 20	1 day	8 hrs	100%		Engineer1	
	Prototype Components Delivered	Wed 7/8/09	Tue 8/4/09 21	20 days	8 hrs	100%		Engineer1[5%]	
_	Review PCB Layout	Tue 9/29/09	Mon 10/5/09 16	5 days	16 hrs	100%			Engineer1[40%]
_	PCB Boards Ordered	Mon 10/19/09		0.5 days	4 hrs	100%			Engineer1
	PCB Boards Received	Mon 10/19/09	Mon 11/9/09 24	15 days	4 hrs	100%			En
,	Specification and Bidding for Outside Assembly	Mon 11/9/09	Thu 11/19/09 25	8 days	8 hrs	100%			
	PCB and Components Sent for Outside Assembly	Thu 11/19/09	Thu 11/19/09 26	0.5 days	4 hrs	100%			
	Prototype Sub-Assemblies Received	Fri 11/20/09	Thu 12/3/09 27	10 days	4 hrs	100%			
	Test and Evaluation of Prototype Sub-Assemblies	Fri 12/4/09	Thu 12/10/09 28	5 days	4 hrs	100%			
	Submission for In-House Final Assembly	Fri 12/11/09	Fri 12/11/09 29	1 day	8 hrs	100%			
	First Prototype Assembly Complete	Tue 12/15/09	Wed 12/16/09 30	2 days	16 hrs	100%			
	Second Prototype Assembly Complete	Fri 12/18/09	Fri 12/18/09 30	1 day	8 hrs	100%			
	Third Prototype Assembly Complete	Wed 2/17/10	Wed 2/17/10 30	1 day	8 hrs	100%			
	DDS VME Prototype Firmware Development	Wed 12/23/09	Fri 9/10/10	188 days	664 hrs	69%			
	Memory Blocks and Data Transfer Infrastructure	Fri 2/19/10	Fri 4/23/10	45.3 days	192 hrs	100%			
;	Layout Memory Map of All Avail. Memory	Fri 2/19/10	Thu 3/11/10	15 days	40 hrs	100%			
	Layout the FPGA M9K Memory Blocks	Fri 2/26/10	Wed 3/3/10 36SS+5 days	3.03 days	8 hrs	100%			
	Design the Inter-FPGA Interface	Wed 3/3/10	Fri 3/19/10 37	12.12 days	32 hrs	100%			
	Design the A32D32 VME Interface	Tue 3/9/10	Tue 3/30/10 38SS+4 days	15.15 days	40 hrs	100%			
	Integrate/Simulate VME, Inter-FPGA and Memory Blocks	Wed 3/17/10	Tue 3/30/10 39SS+6 days	9.09 days	24 hrs	100%			
	Test VME Interface	Tue 3/30/10	Thu 4/15/10 40	12.12 days	32 hrs	100%			
	Flash Memory Interface	Thu 4/15/10	Fri 4/23/10 36,41	6.06 days	16 hrs	100%			
	IO Interface Logic Development	Wed 12/23/09	Mon 9/6/10	184 days	264 hrs	53%			
	LMK01010, Programmable Clock Dist. Setup	Wed 12/30/09	Mon 1/4/10	4 days	16 hrs	100%			
	AD9910, DDS, Setup and Init.	Tue 1/5/10	Mon 1/11/10 44	5 days	40 hrs	100%			
	AD9910, DDS, RF Amplifier Adjustment	Tue 1/12/10	Tue 1/19/10 45	6 days	40 hrs	100%			
_	AD9910, DDS, Multichip Syncronization	Wed 1/20/10	Fri 1/29/10 46	8 days	32 hrs	100%			
	MCP4021, Digital Pot Interface	Mon 8/2/10	Thu 8/5/10 42	4 days	16 hrs	0%			
	AD7625, ADC Interface	Wed 12/23/09		6 days	32 hrs	100%			
	LTC2641, DAC interface	Fri 8/6/10	Fri 8/13/10 48	6 days	32 hrs	0%			
	High-Speed LVDS Intermodule Link	Mon 8/16/10	Mon 8/23/10 50	6 days	16 hrs	0%			
	Rear VME Phase Detector/RSSI Module Interface	Tue 8/24/10	Mon 9/6/10 51	10 days	40 hrs	0%			
	DDS Application Processes Development	Thu 6/24/10	Fri 9/10/10	57 days	208 hrs	40%			
	Shared Memory Management	Thu 6/24/10		5 days	24 hrs	100%			
	10k Point Curve Interpolation	Thu 7/1/10	Wed 7/7/10 54	5 days	24 hrs	100%			
-	Boot-Up Initialization	Thu 7/8/10	Wed 7/14/10 55	5 days	40 hrs	80%			
-	DDS Setup, Syncronization and Verification	Thu 7/15/10	Wed 7/28/10 56	10 days	40 hrs	40%			
-	Run-Mode Freq/Phase Data Processing Task Scheduler and Data Bus Management	Mon 8/16/10 Mon 8/30/10	Fri 8/27/10 57,50 Fri 9/10/10 58	10 days	40 hrs 40 hrs	0% 0%			
-	First Prototype Testing and Evaluation	Thu 12/17/09	Wed 9/1/10 58	10 days 185 days	136 hrs	57%			
-	Power Supply and Distribution Testing	Thu 12/17/09	Thu 12/17/09 31	185 days	8 hrs	100%			
-	DDS Setup and Syncronization Testing	Fri 1/22/10	Fri 1/29/10 47FF	6 days	8 nrs 16 hrs	100%			
-	DDS Setup and Syncronization Testing DDS RF Output Adjustment and Testing	Tue 1/12/10	Tue 1/19/10 46FF	6 days	40 hrs	100%			
+	Analog IO Gain and Offset Calibration	Mon 8/16/10	Fri 8/20/10 50	5 days	24 hrs	0%			
	Analog to Sain and Onset Calibration	191011 0/10/10	1110/20/10 50	J days	24 1115	U /0			
ct: LLR	RF Upgrades Updated Ju Task	Progress		Summary		External Tasks	□ Deadline		
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	Split Inniminimini	Milestone	•	Project Summar	y	External Milesto	ine 🔷		



ID Tas	k Name	Start	Finish	Predecessors	Duration	Work	% Complete	Qtr 4, 2008		Qtr 1, 200	09		Qtr 2, 2009			Qtr 3, 2009			Qtr 4, 20	ງ09
							·		Nov Dec		Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	
65	Analog to Digital Converter Testing and Cal.	Mon 8/23/10	Thu 8/26/10		4 days	16 hrs														
66	Digital to Analog Converter Testing and Cal.	Fri 8/27/10	Wed 9/1/10		4 days	16 hrs														
67	Flash Memory Access Testing	Fri 6/18/10			4 days	16 hrs														
68	Second Prototype Testing and Evaluation	Mon 9/13/10	Fri 10/8/10		19.55 days	84 hrs														
69	Power Supply and Distribution Testing	Mon 9/13/10			1 day	4 hrs														
70	DDS Setup and Syncronization Testing	Tue 9/14/10			6.06 days	16 hrs														
71	DDS RF Output Adjustment and Testing	Wed 9/22/10	Tue 9/28/10		4.82 days	32 hrs														
72	Analog IO Gain and Offset Calibration	Tue 9/28/10	Thu 9/30/10		1.67 days	8 hrs														
73	Analog to Digital Converter Testing and Cal.	Thu 9/30/10	Mon 10/4/10	72	2 days	8 hrs														
74	Digital to Analog Converter Testing and Cal.	Mon 10/4/10	Wed 10/6/10	73	2 days	8 hrs	0%													
75	Flash Memory Access Testing	Wed 10/6/10	Fri 10/8/10	74	2 days	8 hrs	0%													
76	Third Prototype Testing and Evaluation	Fri 10/8/10	Fri 11/5/10		19.55 days	84 hrs	0%													
77	Power Supply and Distribution Testing	Fri 10/8/10	Mon 10/11/10	75	1 day	4 hrs														
78	DDS Setup and Syncronization Testing	Mon 10/11/10			6.06 days	16 hrs														
79	DDS RF Output Adjustment and Testing	Tue 10/19/10			4.82 days	32 hrs														
80	Analog IO Gain and Offset Calibration	Tue 10/26/10			1.67 days	8 hrs														
	Analog to Digital Converter Testing and Cal.				-															
81	0 0	Thu 10/28/10			2 days	8 hrs														
82	Digital to Analog Converter Testing and Cal.	Mon 11/1/10			2 days	8 hrs														
83	Flash Memory Access Testing	Wed 11/3/10	Fri 11/5/10		2 days	8 hrs														
84	Faceplates and Crate Procurement	Fri 11/5/10			5 days	20 hrs														
85	Faceplate Layout	Fri 11/5/10	Mon 11/8/10		1 day	4 hrs														
86	First Piece Faceplate Fabrication Requested	Mon 11/8/10	Tue 11/9/10	85	1 day	4 hrs	0%													
87	First Piece Faceplate Delivered	Tue 11/9/10	Wed 11/10/10	86	1 day	4 hrs	0%													
88	Final Faceplate Fabrication Requested	Wed 11/10/10	Thu 11/11/10		1 day	4 hrs														
89	Final Faceplates Delivered	Thu 11/11/10	Fri 11/12/10	88	1 day	4 hrs														
90	PD_VME_Rear01: Triple Phase Detector, Rear VME Module	Mon 10/19/09	Thu 4/8/10		123 days	272 hrs														_
91	PD_VME Prototype Hardware Development	Mon 10/19/09	Mon 2/22/10		90.5 days	236 hrs													Š	
92	Prototype Design Begins	Mon 10/19/09			0 days	0 hrs														10/
					-															E
93	Initial Design and Layout	Mon 10/19/09			5 days	16 hrs														
94	PCB Parts and Symbol Development	Mon 10/19/09			5 days	8 hrs													=	<u> </u>
95	Schematic Capture and Board Layout	Mon 10/26/09			12 days	40 hrs													ſ	
96	PCB Layout Specification	Mon 11/2/09	Mon 11/16/09	95SS+5 days	10 days	16 hrs													l	4
97	PCB Layout Begins	Mon 11/16/09	Mon 11/16/09	96	0 days	0 hrs														
98	PCB Layout	Mon 11/16/09	Mon 12/14/09	97	20 days	80 hrs	100%													
99	Build BOM and Assembly Parts Database	Mon 11/16/09	Mon 11/23/09	97	5 days	16 hrs	100%													
100	Protoype Component Orders Compiled				2 days	8 hrs														
101	Protoype Components Ordered	Wed 11/25/09			1.25 days	4 hrs														
102	Prototype Components Delivered	Thu 11/26/09			1 day	4 hrs														
103	Review PCB Layout	Mon 12/14/09			-	8 hrs														
	•				3 days															
104	PCB Design Complete		Thu 12/17/09		0 days	0 hrs														
105	PCB Boards Ordered	Mon 12/21/09			1.25 days	4 hrs														
106	PCB Boards Received	Tue 1/5/10	Tue 1/5/10		1 day	4 hrs														
107	Submission for In-House Final Assembly, 3 Modules	Wed 1/6/10	Wed 1/6/10	106	0.5 days	4 hrs														
108	First Prototype Assembly Complete	Fri 1/8/10	Fri 1/8/10	107	1 day	8 hrs	100%													
109	Second Prototype Assembly Complete	Fri 2/19/10	Fri 2/19/10	107	1 day	8 hrs	100%													
110	Third Prototype Assembly Complete	Mon 2/22/10			1 day	8 hrs														
111	First Prototype Testing and Evaluation	Thu 4/1/10	Fri 4/2/10		1.5 days	12 hrs														
112	Power Supply and Distribution Testing	Thu 4/1/10	Thu 4/1/10		0.5 days	4 hrs														
113	AD8307 RSSI Calibration and Testing	Thu 4/1/10	Thu 4/1/10		0.5 days	4 hrs														
					-															
114	AD8302 Phase Detector Calibration and Testing	Fri 4/2/10	Fri 4/2/10		0.5 days	4 hrs														
115	Second Prototype Testing and Evaluation	Fri 4/2/10	Tue 4/6/10		2 days	12 hrs														
116	Power Supply and Distribution Testing	Fri 4/2/10	Fri 4/2/10		0.5 days	4 hrs														
117	AD8307 RSSI Calibration and Testing	Mon 4/5/10	Mon 4/5/10	116	0.5 days	4 hrs														
118	AD8302 Phase Detector Calibration and Testing	Mon 4/5/10	Tue 4/6/10	117	1 day	4 hrs	0%													
119	Third Prototype Testing and Evaluation	Tue 4/6/10	Thu 4/8/10	110	2 days	12 hrs	0%													
120	Power Supply and Distribution Testing	Tue 4/6/10	Tue 4/6/10	118	0.5 days	4 hrs	0%													
121	AD8307 RSSI Calibration and Testing	Wed 4/7/10	Wed 4/7/10		0.5 days	4 hrs														
22	AD8302 Phase Detector Calibration and Testing	Wed 4/7/10	Thu 4/8/10		1 day	4 hrs														
123	RF_Switch_01: RF Switch Module for LLRF Module Online Testing		Tue 12/7/10		384.75 days	356 hrs														
					-															
124	RF Switch Component Evaluation	Wed 6/17/09	Wed 7/1/09		11 days	88 hrs										Enaile				
125	Evaluation Component Procurement	Wed 6/17/09	Tue 6/30/09		10 days	80 hrs										Engineer1				
126	LMH6572 Triple Video Switch Evaluation	Wed 7/1/09			1 day	8 hrs										Engineer1				
127	RF_Switch_01 Prototype Hardware Development		Wed 11/10/10		50.25 days	240 hrs														
128	Initial Design and Layout	Wed 9/1/10	Tue 9/7/10		5 days	16 hrs	0%													
	Task	Deserve			Cum			stornel T!			adline.	п								_
	RF Upgrades Updated Ju Task	Progress			Summary	_		kternal Tasks		Dea	adline	企								
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roject: LL ate: Wed	7/21/10 Split	Milestone	•		Project Summa	ary 🔍		xternal Milesto	ne 🔷											



ID T	ask Name	Start	Finish F	Predecessors	Duration	Work 9	% Complete Qtr 4, 2008	Qtr 1, 2009	Qtr 2, 2009	Qtr 3, 2009	Qtr 4, 2009
129	Schematic Capture and Board Layout	Wed 9/8/10	Thu 9/9/10	128	2 days	8 hrs	Oct Nov	Dec Jan Feb Mar	Apr May Jun	Jul Aug Sep	Oct Nov
130	Initial Component Procurement	Wed 9/8/10		128	1.25 days	4 hrs	0%				
131	PCB Layout Specification	Fri 9/10/10	Thu 9/23/10	129	10 days	40 hrs	0%				
132	PCB Parts and Symbol Development	Fri 9/24/10	Mon 9/27/10	131	2 days	16 hrs	0%				
133	Ready to Begin PCB Layout	Mon 9/27/10	Mon 9/27/10	132	0 days	0 hrs	0%				
134	PCB Layout	Tue 9/28/10	Mon 10/25/10	133	20 days	80 hrs	0%				
135	Build BOM and Assembly Parts Database	Tue 9/28/10	Mon 10/4/10	133	5 days	16 hrs	0%				
136	Protoype Component Orders Compiled	Tue 10/5/10	Wed 10/6/10	135	2 days	8 hrs	0%				
137	Protoype Components Ordered	Thu 10/7/10		136	1.25 days	4 hrs	0%				
138	Prototype Components Received		Mon 10/11/10	137	1 day	4 hrs	0%				i
139	Review PCB Layout		Thu 10/28/10	134	2.5 days	8 hrs	0%				
140	PCB Design Complete		Thu 10/28/10	139	0 days	0 hrs	0%				
141	PCB Boards Descript	Thu 10/28/10		140	1.25 days	4 hrs	0% 0%				
142	PCB Boards Received Submission for In-House Final Assembly, 3 Modules	Fri 10/29/10 Mon 11/1/10		141	1 day 0.5 days	4 hrs	0%				
143	First Prototype Assembly Complete	Tue 11/2/10		142 143	-	8 hrs	0%				
145	Second Prototype Assembly Complete	Thu 11/4/10		143	2 days 2 days	8 hrs	0%				
146	Third Prototype Assembly Complete		Wed 11/10/10	145	2 days	8 hrs	0%				
147	First Prototype Testing and Evaluation	Thu 11/4/10		143	23.5 days	28 hrs	0%				
148	Power Supply and Distribution Testing	Thu 11/4/10		144	0.5 days	4 hrs	0%				
149	RF Switch Propagation Delay Measurement	Thu 11/4/10		148	1 day	8 hrs	0%				
150	RF Switch Testing Short Term	Fri 11/5/10		149	2 days	8 hrs	0%				
151	RF Switch Testing Long Term	Tue 11/9/10		150	20 days	8 hrs	0%				
152	LLRF Module Development and Testing User Interface	Mon 3/22/10		100	156.24 days	608 hrs	7%				
153	USB Serial and VME Processor Interface Development		Tue 10/26/10		156.24 days	608 hrs	7%				
154	Establish Software Development Test Bench	Mon 3/22/10			10 days	40 hrs	60%				
155	Setup/Network PC for USB Interface	Mon 3/22/10			1 day	4 hrs	100%				i
156	Install PD_VME Module and BLLRF Processor Node	Tue 3/23/10	Wed 3/24/10	155	2 days	8 hrs	100%				
157	Install USB-FIFO Drivers for program Development	Thu 3/25/10	Thu 3/25/10	156	1 day	4 hrs	100%				
158	Install and Configure Programming IDE	Fri 3/26/10	Mon 3/29/10	157	2 days	8 hrs	100%				
159	Establish Programming Environment for BLLRF Node	Tue 3/30/10	Fri 4/2/10	158	4 days	16 hrs	0%				
160	Develop Front VME Module for Testing Interfaces	Tue 3/23/10	Wed 4/21/10		21.24 days	32 hrs	28%				
161	Modify Older VME Module to Interface with	Tue 3/23/10	Wed 3/24/10	155	2 days	8 hrs	100%				
162	Design, Write and Test FPGA Logic for USB Interface	Thu 3/25/10	Tue 3/30/10	161	4 days	8 hrs	20%				
163	Adapt and Test FPGA Logic for VME Interface	Thu 4/15/10	Wed 4/21/10	41,162	4 days	16 hrs	0%				i
164	Test Interface Software Development	Wed 4/21/10	Tue 10/26/10		134 days	536 hrs	1%				
165	LLRF Module Test Application Specification	Wed 4/21/10			16 days	64 hrs	13%				
166	Specification of Memory Maps and Data Access	Wed 4/21/10		163	4 days	16 hrs	0%				
167	Specification of Module Function Tests	Tue 4/27/10		166	4 days	16 hrs	0%				
168	Specification of User Interface	Mon 5/3/10		167	4 days	16 hrs	50%				
169	Specification of Data File Management	Fri 5/7/10		168	4 days	16 hrs	0%				
170	LLRF Module Field Monitor Application Specification			400	8 days	32 hrs	0%				
171	Specification of Functions	Thu 5/13/10		169	4 days	16 hrs	0%				i
172	Write User Documentation	Wed 5/19/10		171	4 days	16 hrs	0%				
173	Software Written and Tested		Tue 10/26/10 Tue 7/20/10	170	110 days	440 hrs	0%				
174 175	Write Software, version 1 Test Software, version 1	Tue 5/25/10 Tue 7/20/10		172 174	40 days 10 days	160 hrs 40 hrs	0% 0%				
176	Write Software, version 2	Tue 7/20/10		174	20 days	80 hrs	0%				
177	Test Software, version 2	Tue 8/31/10		175	10 days	40 hrs	0%				
178	Write Software, version 3		Tue 10/12/10	177	20 days	80 hrs	0%				
179	Test Software, version 3		Tue 10/12/10	177	10 days	40 hrs	0%				
180	LLRF On-Line System Testing	Fri 10/1/10		170	391 days	1,240 hrs	0%				
181	Test System Hardware Development	Fri 10/1/10			95 days	424 hrs	0%				
182	Development of System Integration Hardware		Thu 11/25/10		40 days	240 hrs	0%				
183	Installation of System Integration Hardware	Fri 11/26/10		182	20 days	80 hrs	0%				
184	Testing of System Integration Hardware	Fri 12/24/10		183	10 days	40 hrs	0%				
185	Installation of New VME Crate	Fri 1/7/11	Thu 1/13/11	184	5 days	24 hrs	0%				
186	Off-Line Testing of New Modules	Fri 1/14/11	Thu 2/10/11	185	20 days	40 hrs	0%				
187	Single Booster Cycle Testing	Fri 2/11/11	Fri 8/19/11		136 days	496 hrs	0%				
188	New Phase Detector Only Testing	Fri 2/11/11	Tue 2/15/11	186	2.67 days	16 hrs	0%				
189	New Frequency Source Only Testing	Tue 2/15/11	Tue 3/15/11	188	20 days	80 hrs	0%				
190	New Main Injector Phase Lock Testing	Tue 3/15/11	Tue 5/10/11	189	40 days	160 hrs	0%				
191	New Frequency Source and New Phase Control Testing	Tue 5/10/11	Fri 6/24/11	190	33.33 days	160 hrs	0%				
192	Full Freq., Phase, and MI Phase Lock Testing	Mon 6/27/11	Fri 8/19/11	191	40 days	80 hrs	0%				<u> </u>
Droin et l	LRF Upgrades Updated Ju Task	Progress			Summary		External Tasks	Deadline			
	od 7/21/10	Milantana			•	·		- Dodding V			
	Split Split	Milestone	•		Project Summar	у	External Milestone ♦				
			·				Page 3				



Task	Name		Start	Finish Pred	decessors	Duration	Work	% Complete Qtr 4, 2008 Oct Nov	Qtr 1, 2009 Dec Jan Feb	Qtr 2, 2009 Mar Apr May	Utr 3, 2009 Jun Jul Aug	Qtr 4, 2009 Sep Oct Nov
	Long Term Testing by	AD Operations	Mon 8/22/11	Fri 3/30/12		160 days	320 hrs	0%	Dec Jan Feb	iviai Api Way	Jul Aug	Jep Oct INOV
	Phase I Testing		Mon 8/22/11	Fri 12/9/11	192 194	80 days	160 hrs					
	Phase II Testing		Mon 12/12/11	Fri 3/30/12	194	80 days	160 hrs	0%				
115	E Unarados — Undatad III	Task	Progress		j	Summary		External Tasks	Deadline	Ŷ		
LLR ed 7/	RF Upgrades Updated Ju 7/21/10								Deauille	V		
		Split	 ivillestone	•		Project Summary		External Milestone ♦				
								Page 4				

