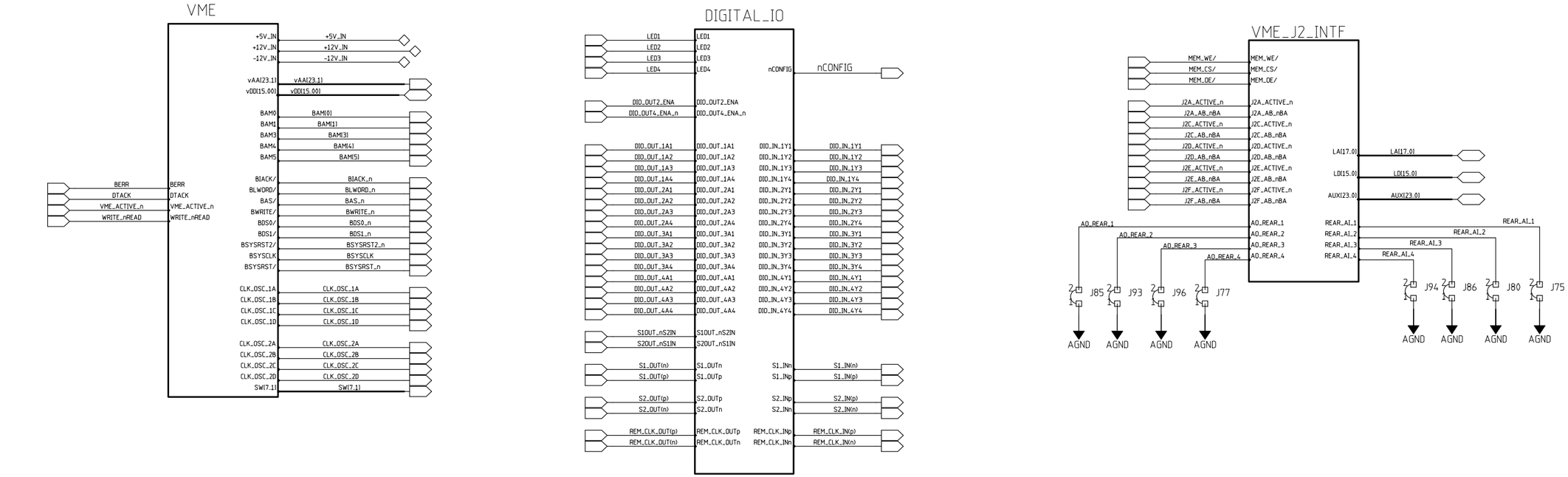

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EED Department	ORIGINATOR	originator	DATE date
	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
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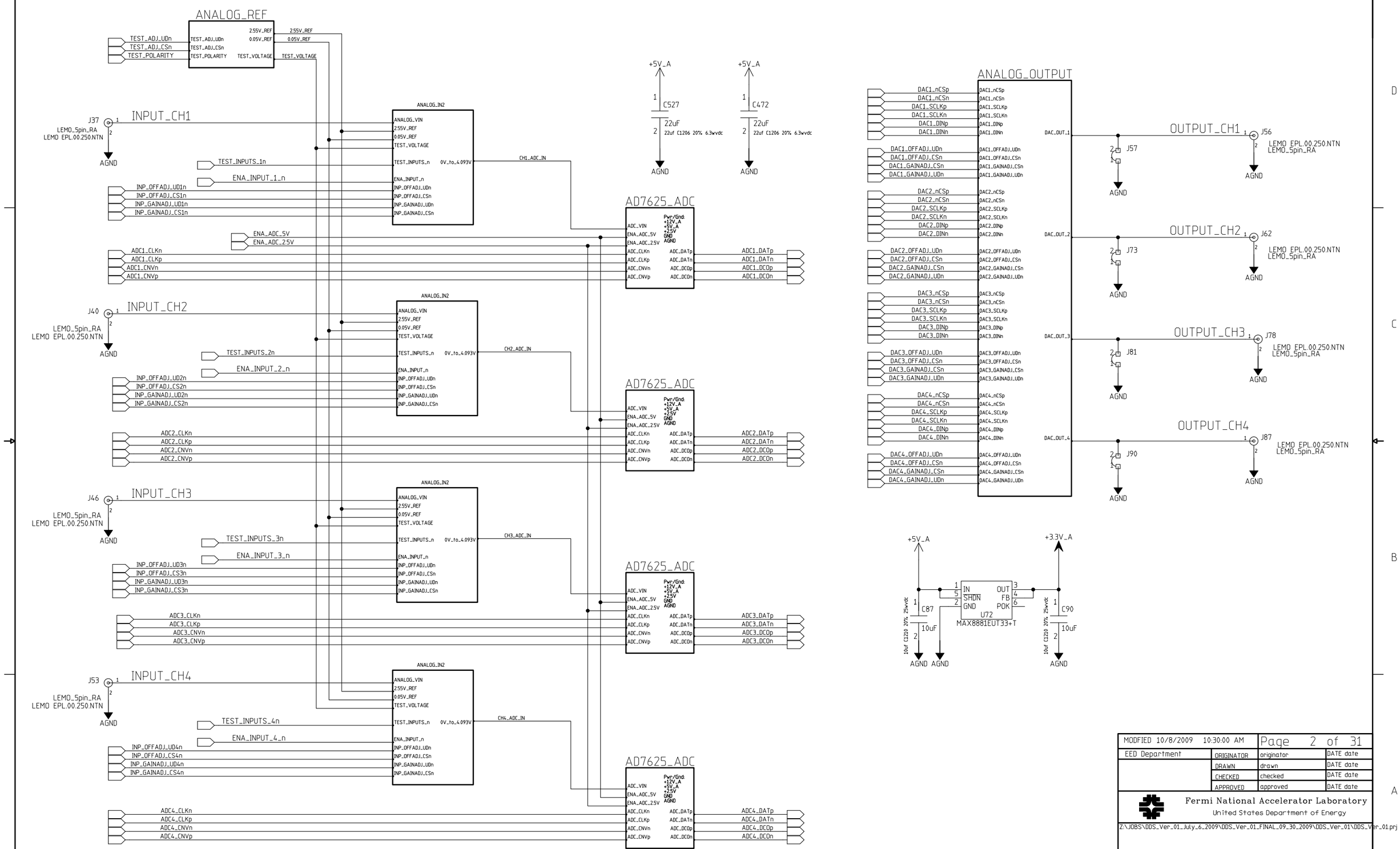
D	drawing number	A

Schematic Page 01 of 09

H=BND; V=4LA



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D	drawing number	A

Schematic Page 02 of 09

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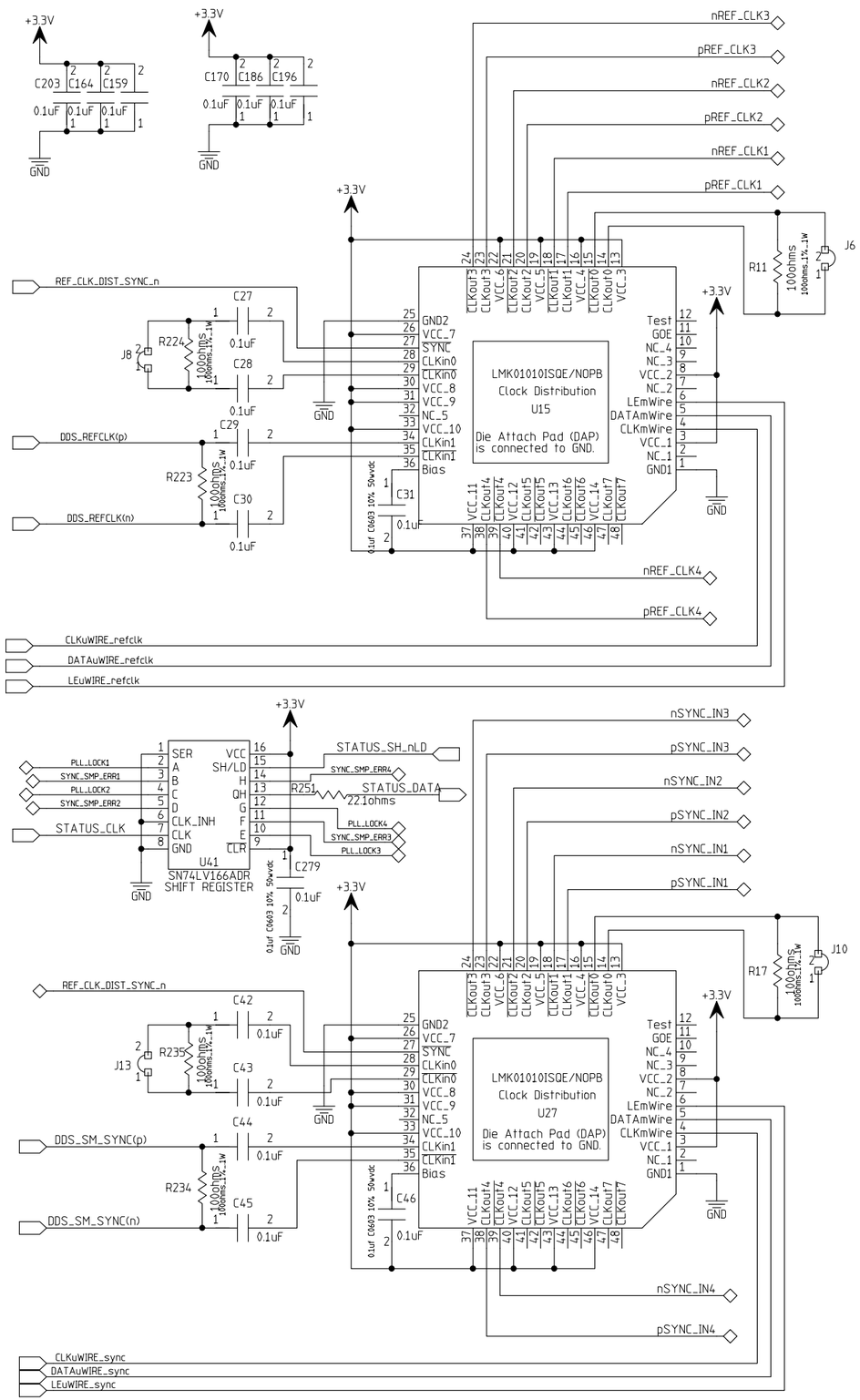

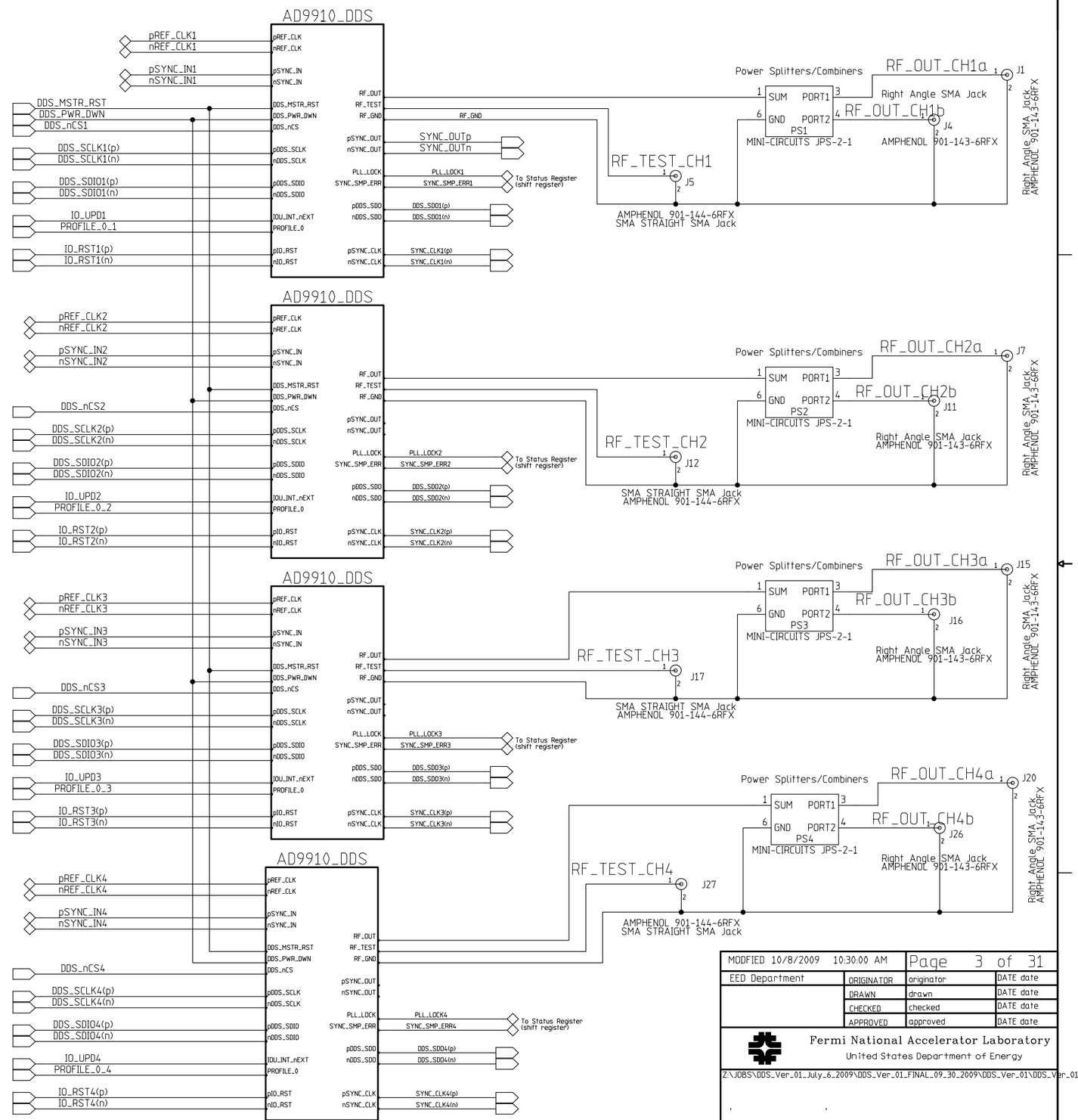

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SIZE	DRAWING NUMBER	REV
D	drawing number	A

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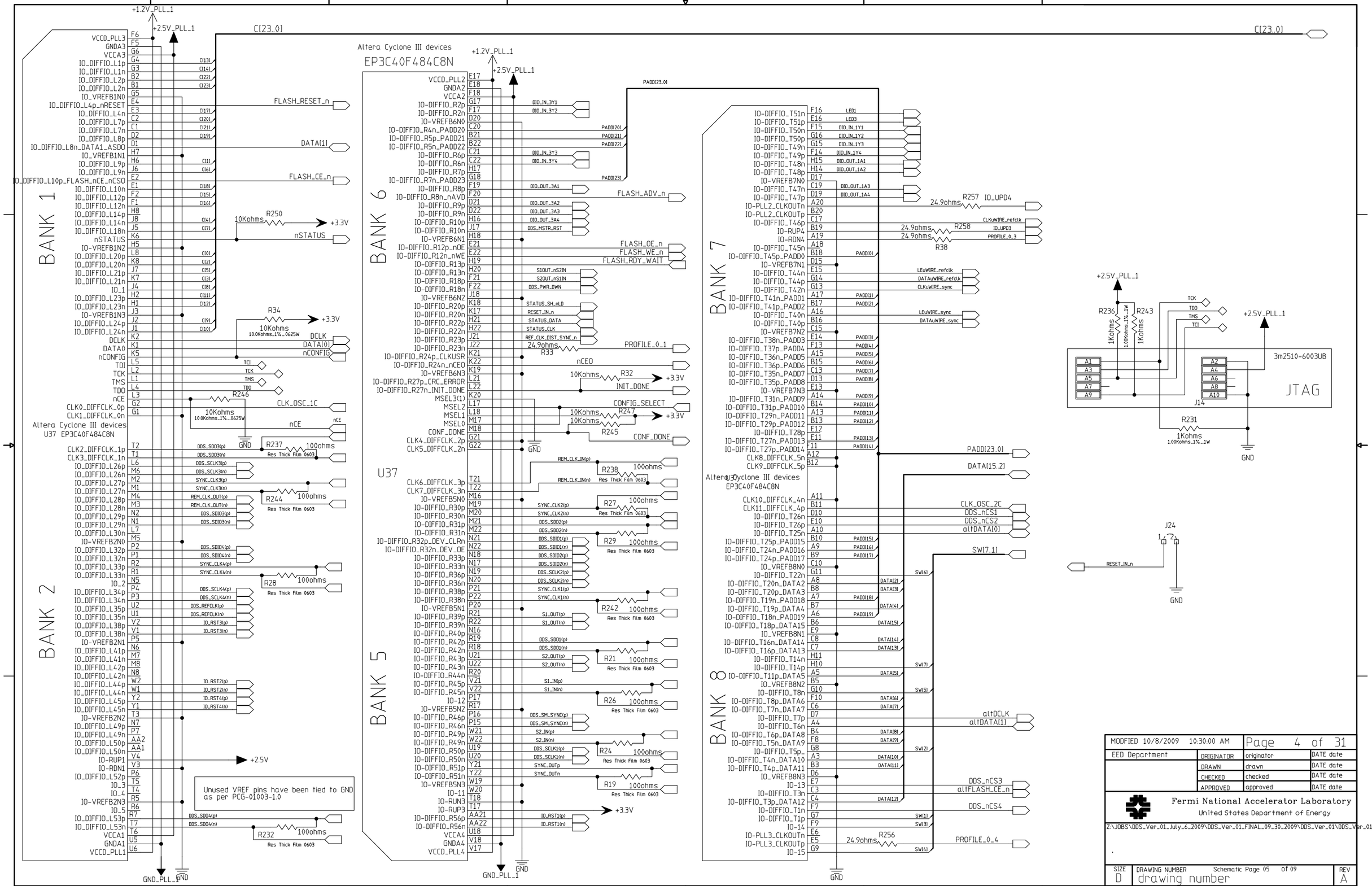
BANK 1
BANK 2
BANK 5
BANK 6
BANK 7
BANK 8
Altera Cyclone III devices
EP3C40F484C8N
U37
C[23..0]
FLASH_RESET_n
DATA[1]
FLASH_CE_n
nSTATUS
DCLK
DATA[0]
nCONFIG
TCI
TCK
TMS
TDO
nCE
CLK_OSC_1C
CLK2_DIFFCLK_1p
CLK3_DIFFCLK_1n
CLK6_DIFFCLK_3p
CLK7_DIFFCLK_3n
CLK10_DIFFCLK_4n
CLK11_DIFFCLK_4p
CLK8_DIFFCLK_5n
CLK9_DIFFCLK_5p
FLASH_ADV_n
FLASH_OE_n
FLASH_WE_n
FLASH_RDY_WAIT
PROFILE_0_1
CONF_DONE
INIT_DONE
PADD[23.0]
DATA[15..2]
CLK_OSC_2C
DDS_nCS1
DDS_nCS2
altDATA[0]
SW[7..1]
altDCLK
altDATA[1]
DDS_nCS3
altFLASH_CE_n
DDS_nCS4
PROFILE_0_4
IO_UPD4
CLKUWIRE_refclk
IO_UPD3
PROFILE_0..3
LEUWIRE_refclk
DATAUWIRE_refclk
CLKUWIRE_sync
LEUWIRE_sync
DATAUWIRE_sync
R250 10Kohms
R34 10Kohms 10.0Kohms_1%_.0625W
R246 10Kohms 10.0Kohms_1%_.0625W
R237 100ohms Res Thick Film 0603
R244 100ohms Res Thick Film 0603
R28 100ohms Res Thick Film 0603
R232 100ohms Res Thick Film 0603
R33 24.9ohms
R32 10Kohms
R247 10Kohms
R245 10Kohms
R238 100ohms Res Thick Film 0603
R27 100ohms Res Thick Film 0603
R29 100ohms Res Thick Film 0603
R242 100ohms Res Thick Film 0603
R21 100ohms Res Thick Film 0603
R26 100ohms Res Thick Film 0603
R24 100ohms Res Thick Film 0603
R19 100ohms Res Thick Film 0603
R257 24.9ohms
R258 24.9ohms
R38 24.9ohms
R256 24.9ohms
R236 1Kohms 1.00Kohms_1%_.1W
R243 1Kohms 1.00Kohms_1%_.1W
R231 1Kohms 1.00Kohms_1%_.1W
3m2510-6003UB
JTAG
J14
J24
RESET_IN_n
+1.2V_PLL_1
+2.5V_PLL_1
+3.3V
+2.5V
GND
GND_PLL_1
Unused VREF pins have been tied to GND as per PCG-01003-1.0
MODIFIED 10/8/2009 10:30:00 AM
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EED Department
ORIGINATOR originator DATE date
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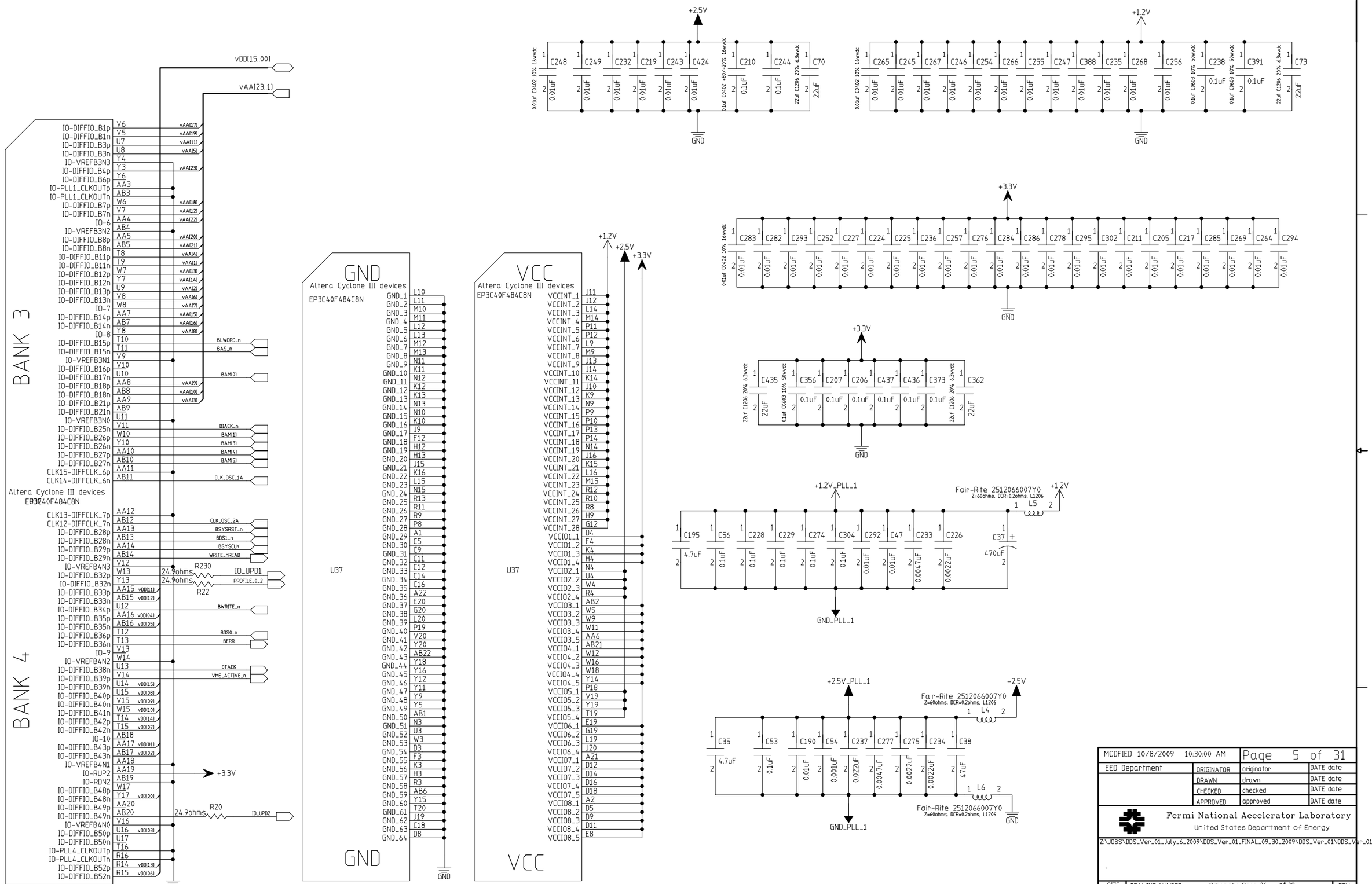
SIZE D
DRAWING NUMBER Schematic Page 05 of 09
drawing number
REV A
H=8ND, V=4LA



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SIZE	DRAWING NUMBER	REV
D	drawing number	A

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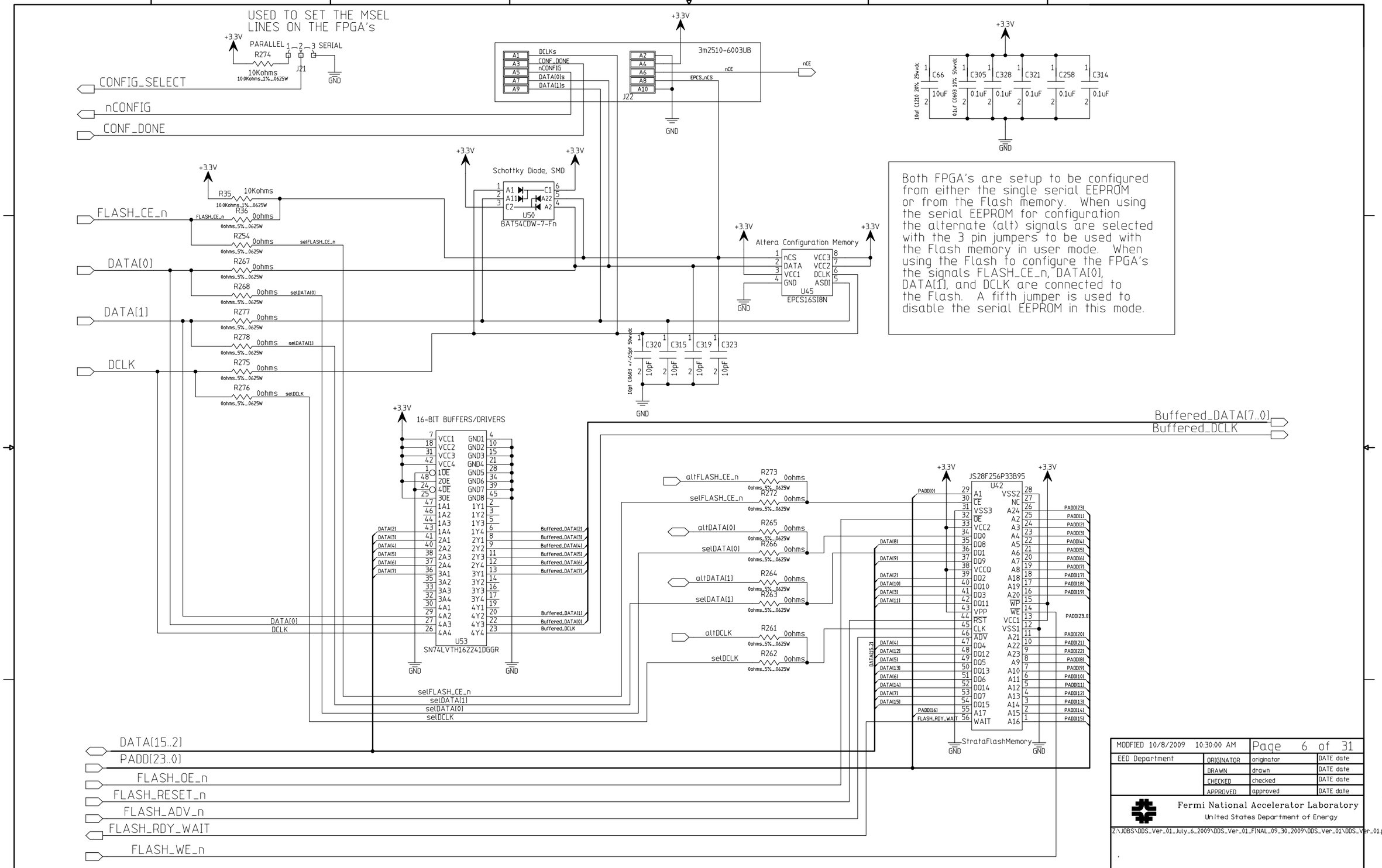

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SIZE	DRAWING NUMBER	REV
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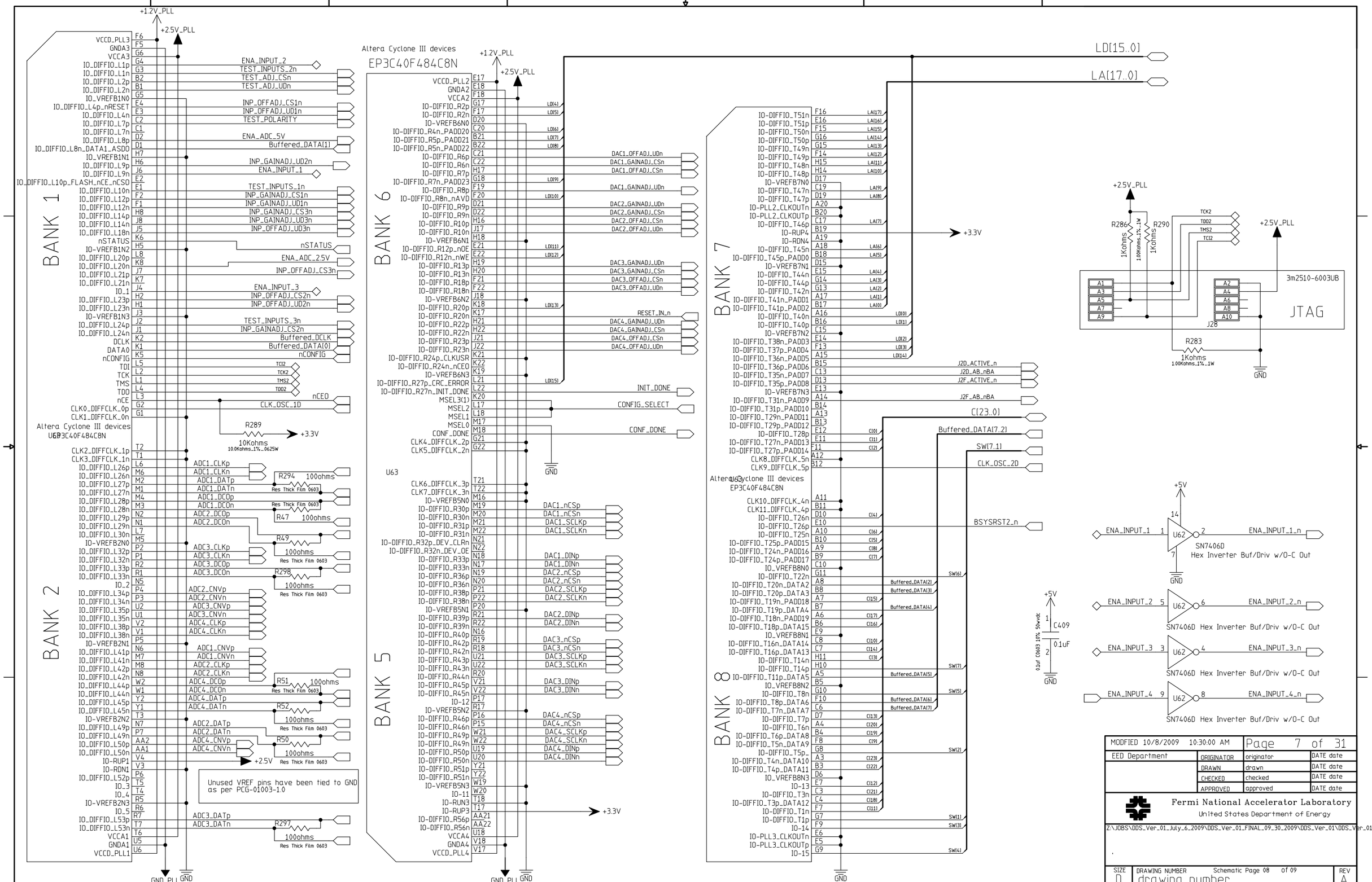
H:8ND, V:4LA


BANK 1
BANK 2
BANK 5
BANK 6
BANK 7
BANK 8
Altera Cyclone III devices
EP3C40F484C8N
U63
U62
JTAG
3m2510-6003UB
J28
SN7406D
Hex Inverter Buf/Driv w/O-C Out
LD[15..0]
LA[17..0]
C[23..0]
Buffered_DATA[7..2]
SW[7..1]
CLK_OSC_2D
BSYSRST2_n
J2D_ACTIVE_n
J2D_AB_nBA
J2F_ACTIVE_n
J2F_AB_nBA
INIT_DONE
CONFIG_SELECT
CONF_DONE
RESET_IN_n
nSTATUS
nCONFIG
nCEO
CLK_OSC_1D
Buffered_DCLK
Buffered_DATA[0]
Buffered_DATA[1]
ENA_ADC_5V
ENA_ADC_2.5V
ENA_INPUT_1
ENA_INPUT_2
ENA_INPUT_3
ENA_INPUT_1_n
ENA_INPUT_2_n
ENA_INPUT_3_n
ENA_INPUT_4_n
+1.2V_PLL
+2.5V_PLL
+3.3V
+5V
GND
GND_PLL
R289 10Kohms 10.0Kohms_1%_.0625W
R294 100ohms
R47 100ohms
R49 100ohms
R298 100ohms
R51 100ohms
R52 100ohms
R50 100ohms
R297 100ohms
Res Thick Film 0603
Unused VREF pins have been tied to GND as per PCG-01003-1.0
R286 1Kohms 100Kohms_1%_1W
R290 1Kohms 100Kohms_1%_1W
R283 1Kohms 100Kohms_1%_1W
C409 0.1uF C0603 10% 50Vvdc
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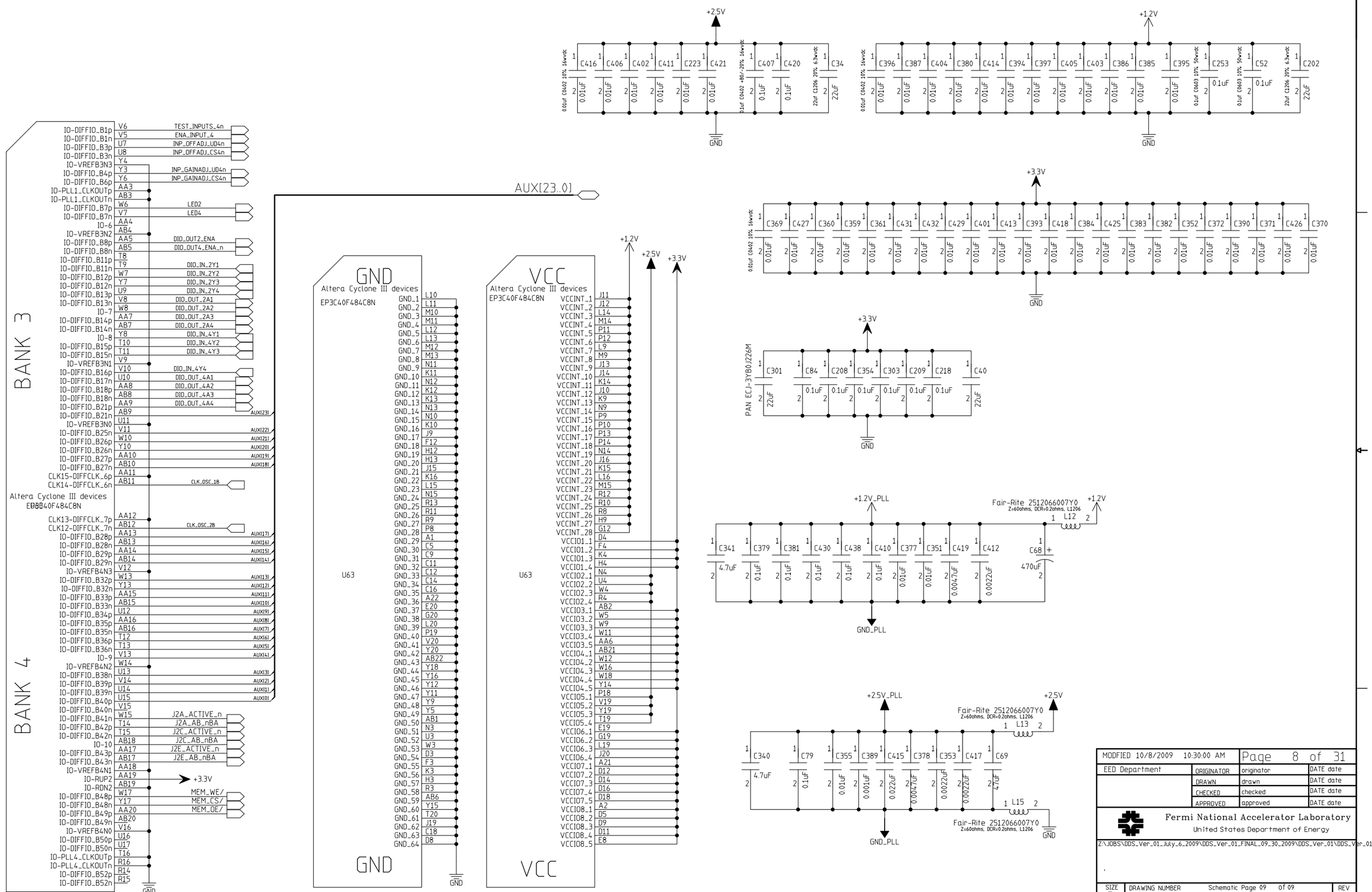
SIZE D
DRAWING NUMBER Schematic Page 08 of 09
drawing number
REV A
H=8ND, V=4LA



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SIZE	DRAWING NUMBER	REV
D	drawing number	A

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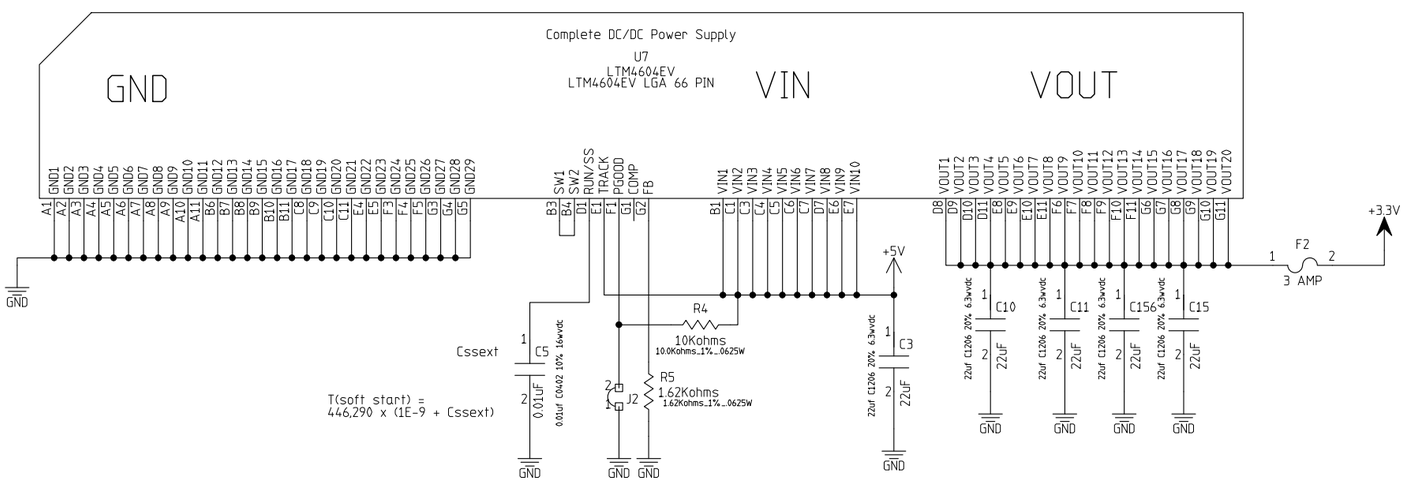

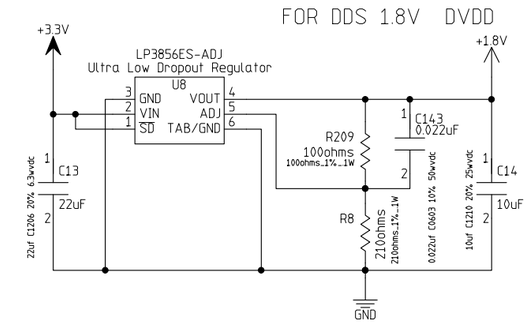

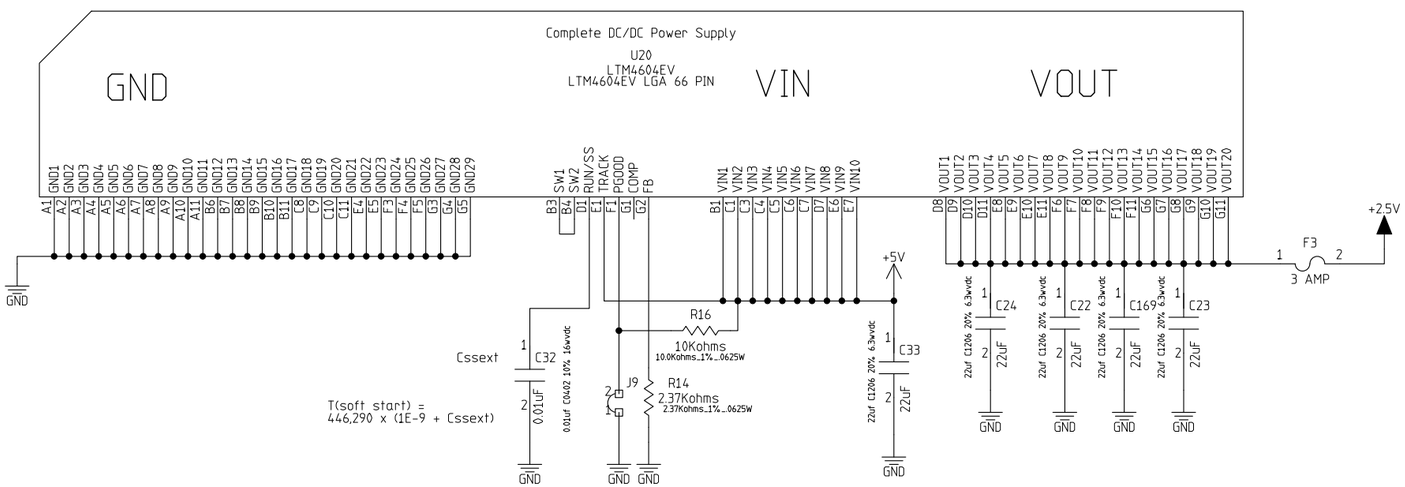

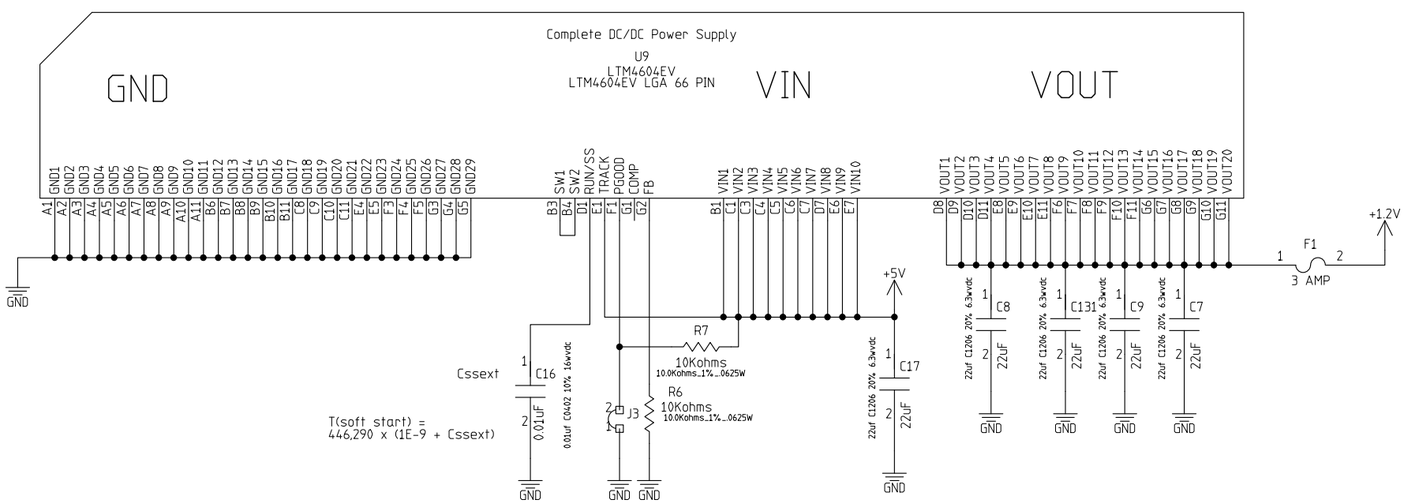

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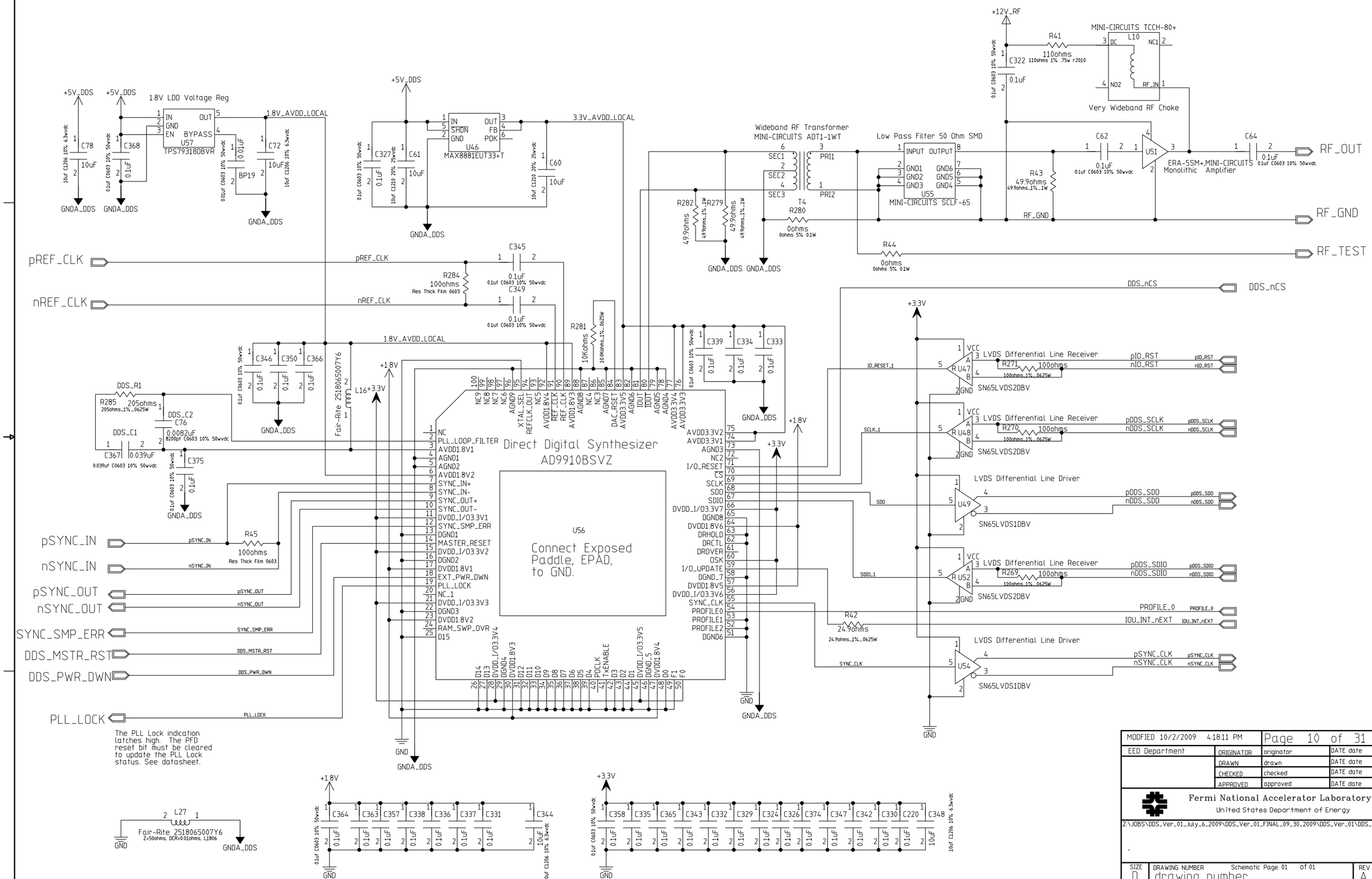
H=BND; V=4LA


1.8V LDO Voltage Reg
U57
TPS79318DBVR
U46
MAX8881EUT33+T
Direct Digital Synthesizer
AD9910BSVZ
U56
Connect Exposed Paddle, EPAD, to GND.
Wideband RF Transformer
MINI-CIRCUITS ADT1-1WT
T4
MINI-CIRCUITS TCCH-80+
Very Wideband RF Choke
Low Pass Filter 50 Ohm SMD
U55
MINI-CIRCUITS SCLF-65
U51
ERA-5SM+,MINI-CIRCUITS Monolithic Amplifier
RF_OUT
RF_GND
RF_TEST
pREF_CLK
nREF_CLK
pSYNC_IN
nSYNC_IN
pSYNC_OUT
nSYNC_OUT
SYNC_SMP_ERR
DDS_MSTR_RST
DDS_PWR_DWN
PLL_LOCK
DDS_nCS
LVDS Differential Line Receiver
LVDS Differential Line Driver
SN65LVDS2DBV
SN65LVDS1DBV
U47
U48
U49
U52
U54
pIO_RST
nIO_RST
pDDS_SCLK
nDDS_SCLK
pDDS_SDO
nDDS_SDO
pDDS_SDIO
nDDS_SDIO
PROFILE_0
IOU_INT_nEXT
pSYNC_CLK
nSYNC_CLK
The PLL Lock indication latches high. The PFD reset bit must be cleared to update the PLL Lock status. See datasheet.
L27
Fair-Rite 2518065007Y6
Z=50ohms, DCR=0.01ohms, L1806
MODIFIED 10/2/2009 4:18:11 PM
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EED Department
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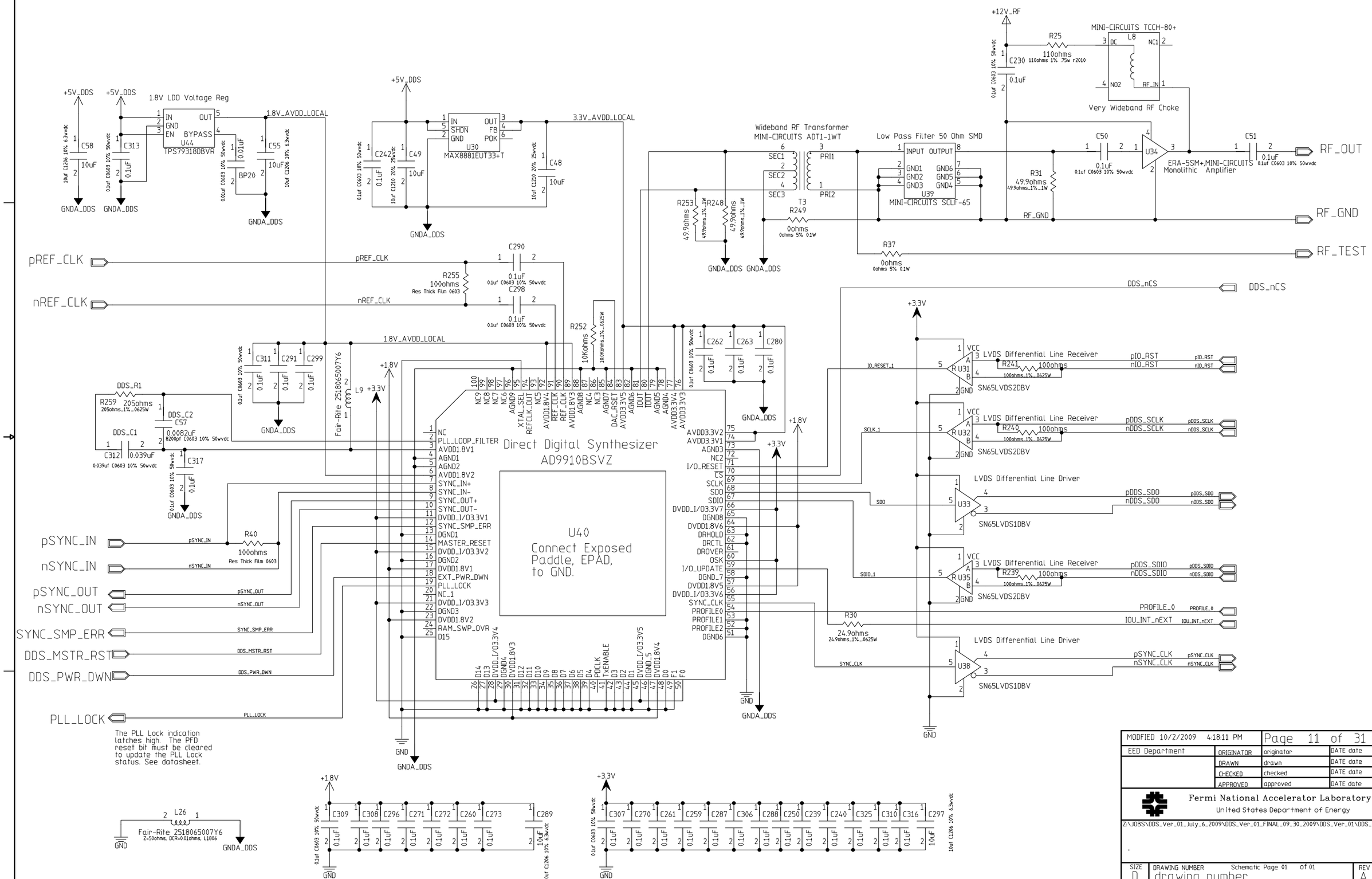
DRAWING NUMBER drawing number
Schematic Page 01 of 01
REV A



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SIZE	DRAWING NUMBER	REV
D	drawing number	A

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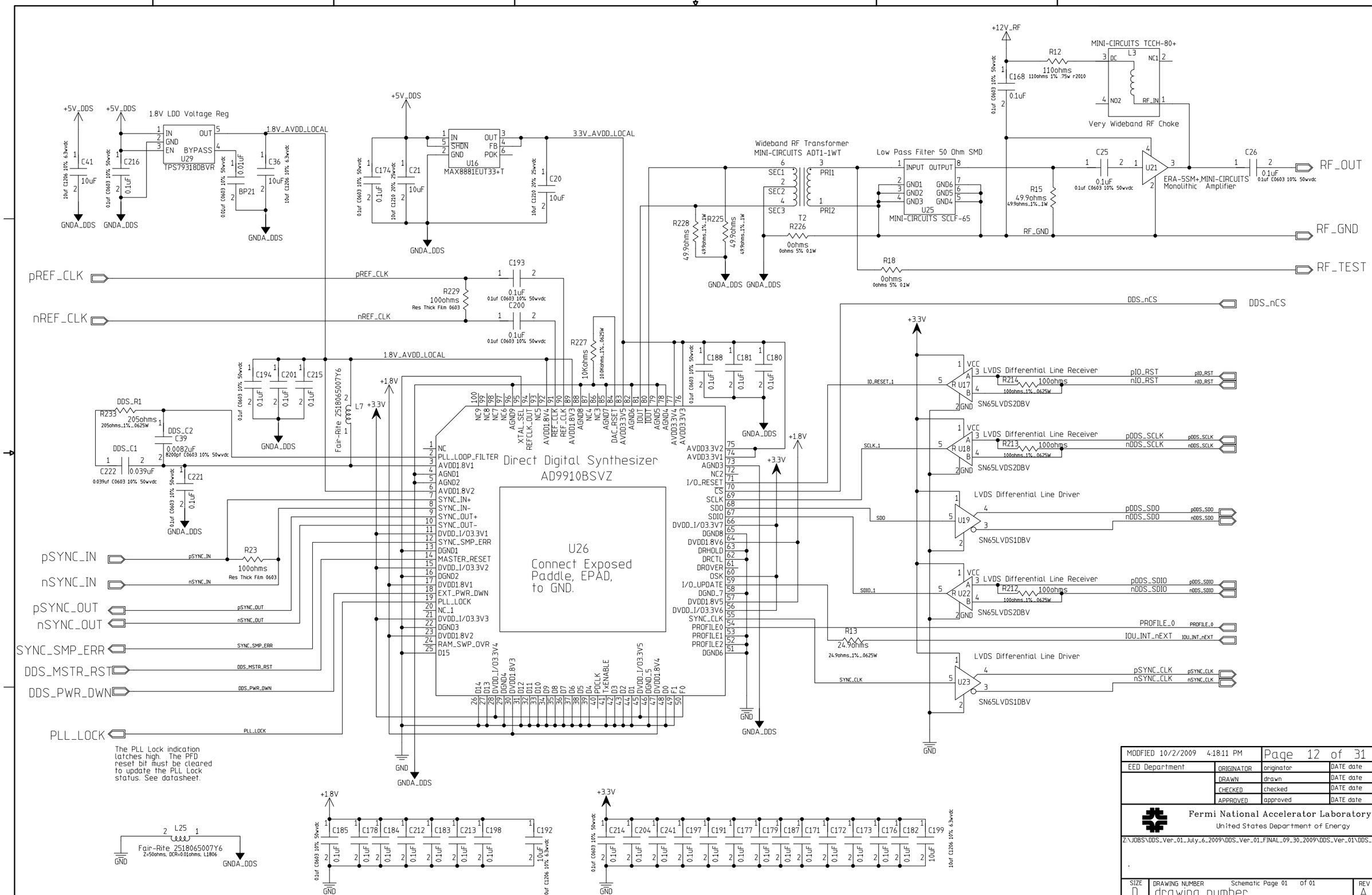

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SIZE	DRAWING NUMBER	REV
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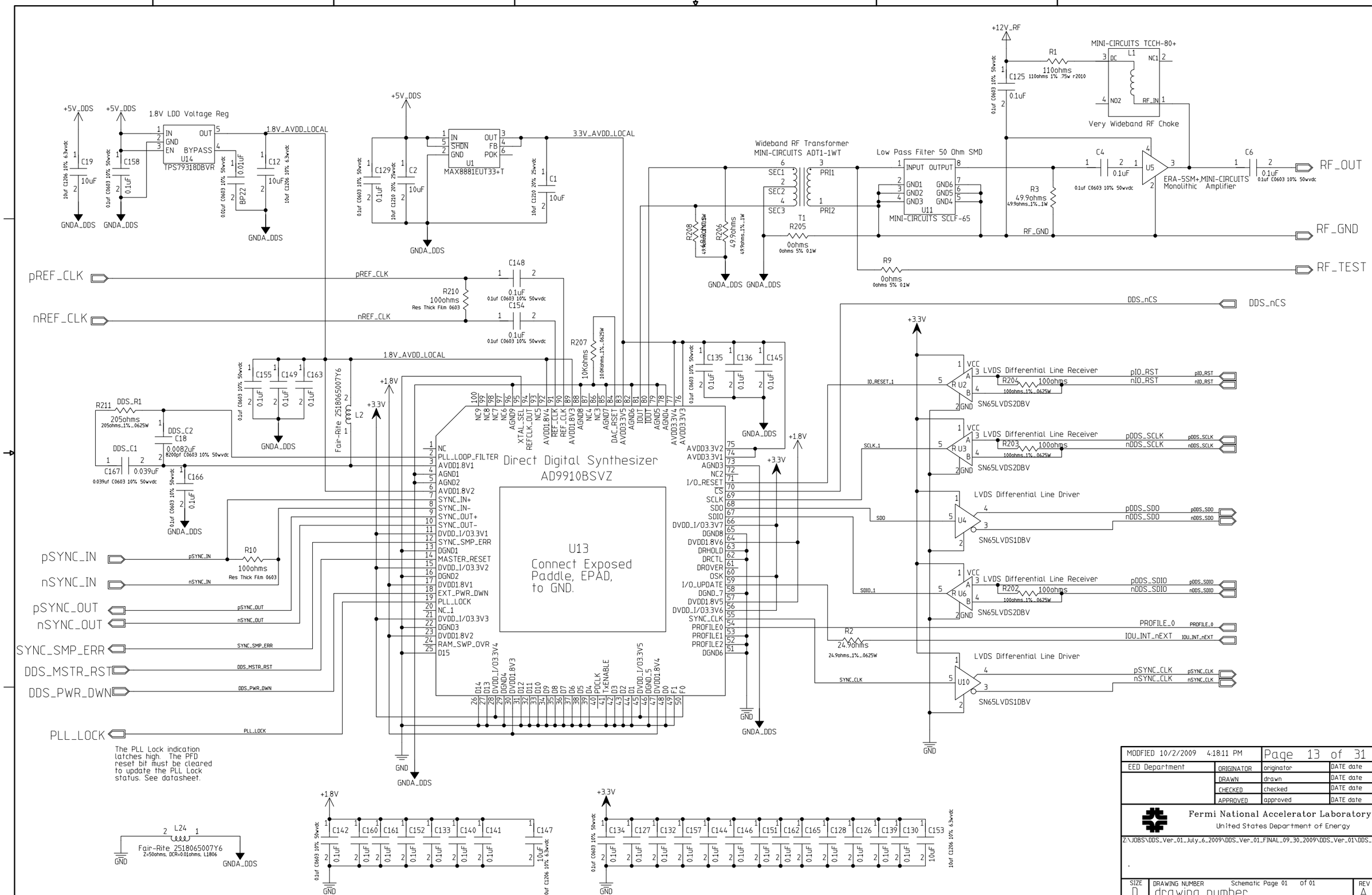

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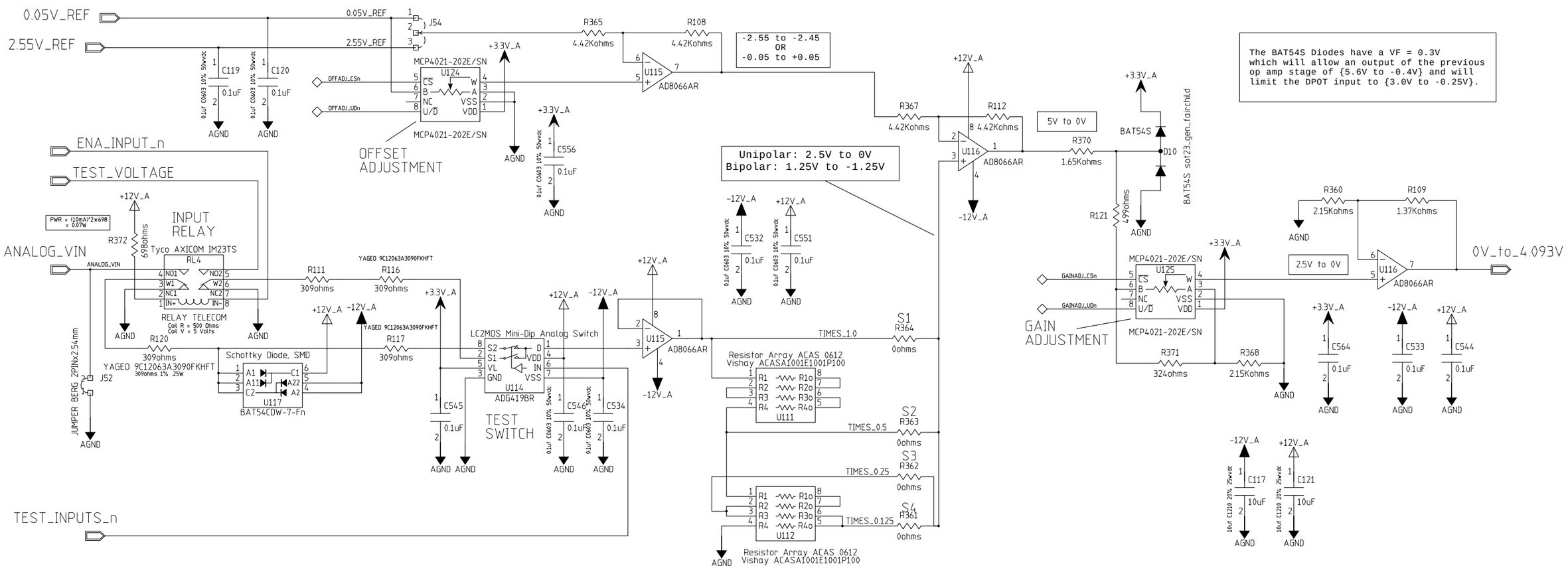
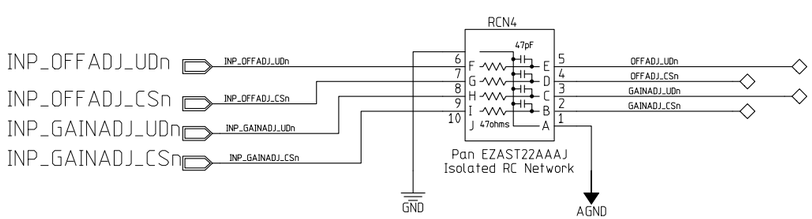
H=BND, V=4LA





Simple Range Selection		
Volts	Input Range	Install
+10	to -10	S4
+5	to -5	S3
+2.5	to -2.5	S2
+1.25	to -1.25	S1
+10	to 0	S3
+5	to 0	S2
+2.5	to 0	S1

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SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	A

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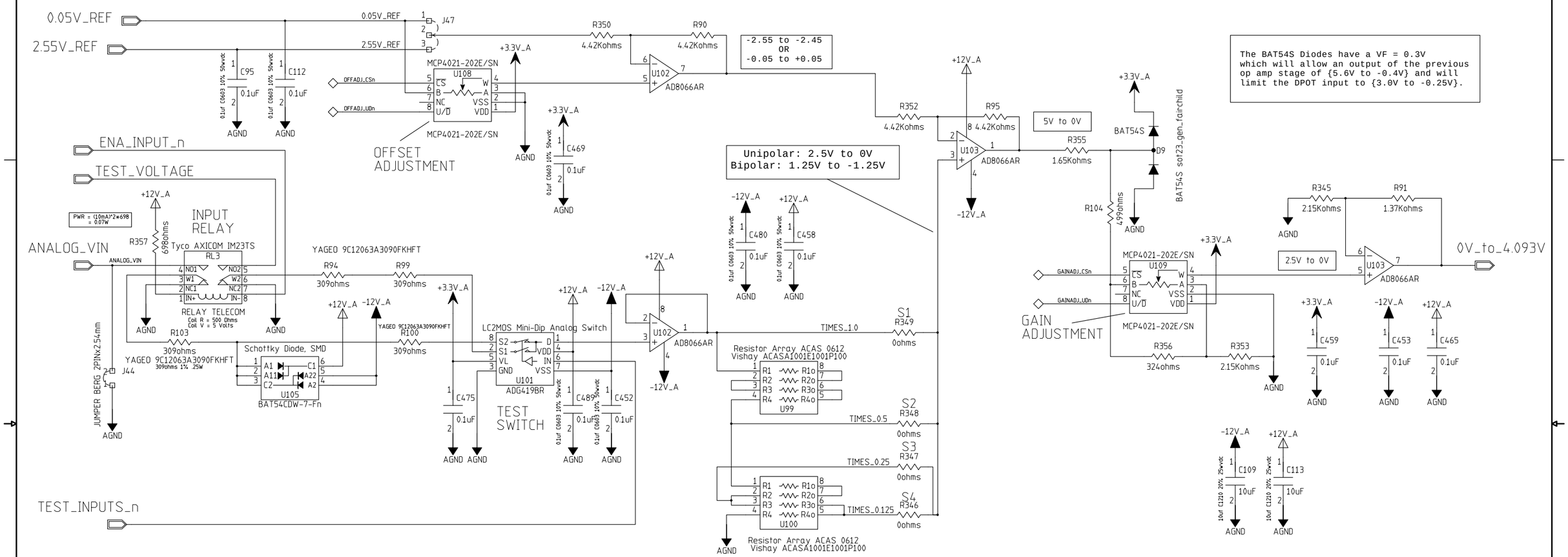

Simple Range Selection		
Volts	Input Range	Install
+10	to -10	S4
+5	to -5	S3
+2.5	to -2.5	S2
+1.25	to -1.25	S1
+10	to 0	S3
+5	to 0	S2
+2.5	to 0	S1

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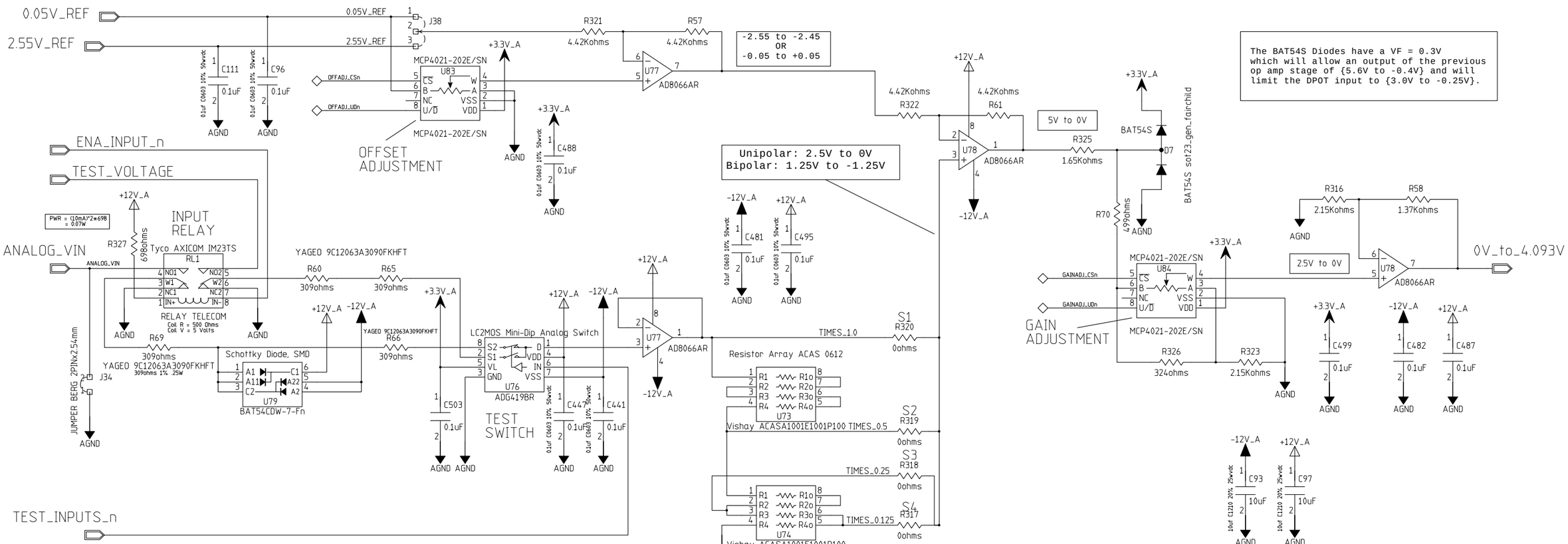

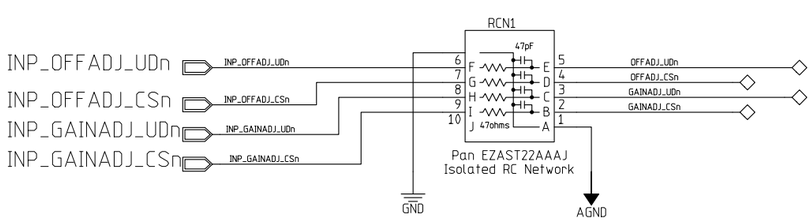

Simple Range Selection

Volts	Input Range	Install
+10	to -10	S4
+5	to -5	S3
+2.5	to -2.5	S2
+1.25	to -1.25	S1
+10	to 0	S3
+5	to 0	S2
+2.5	to 0	S1

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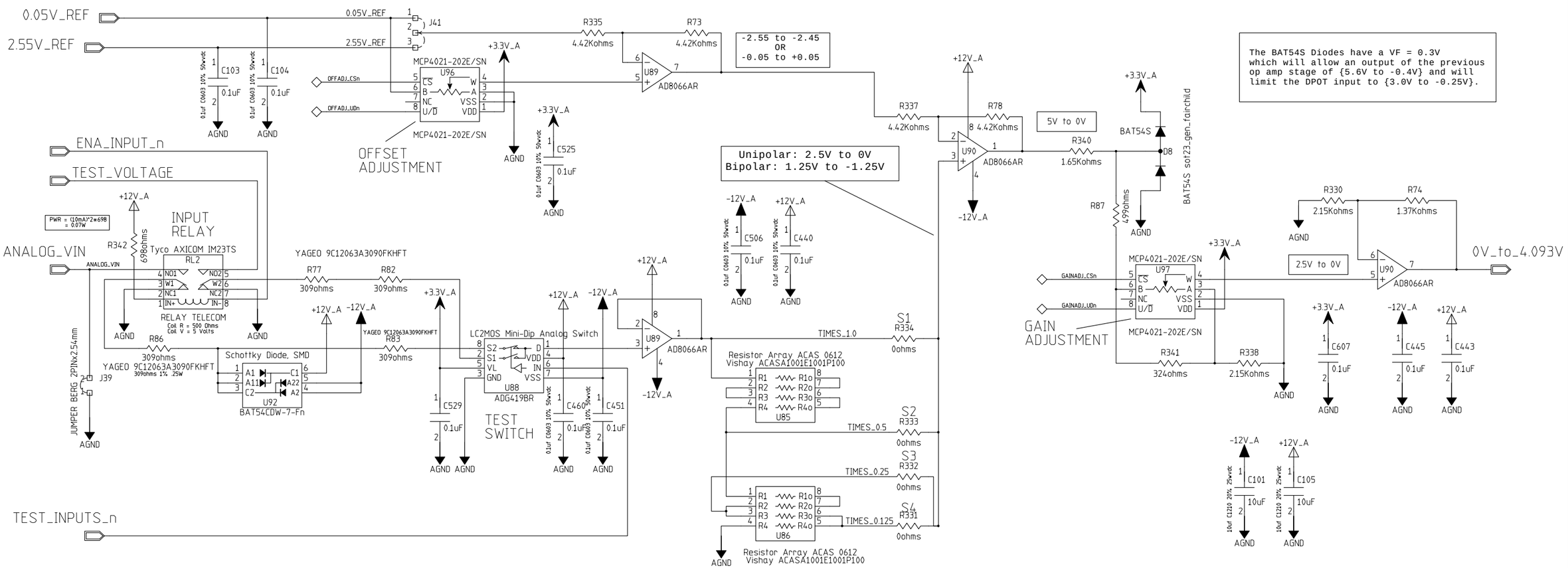

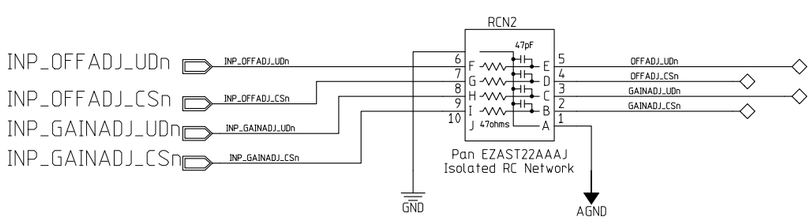

Simple Range Selection

Volts	Input Range	Install
+10	to -10	S4
+5	to -5	S3
+2.5	to -2.5	S2
+1.25	to -1.25	S1
+10	to 0	S3
+5	to 0	S2
+2.5	to 0	S1

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D	drawing number (Schematic Page 01 of 01)	A

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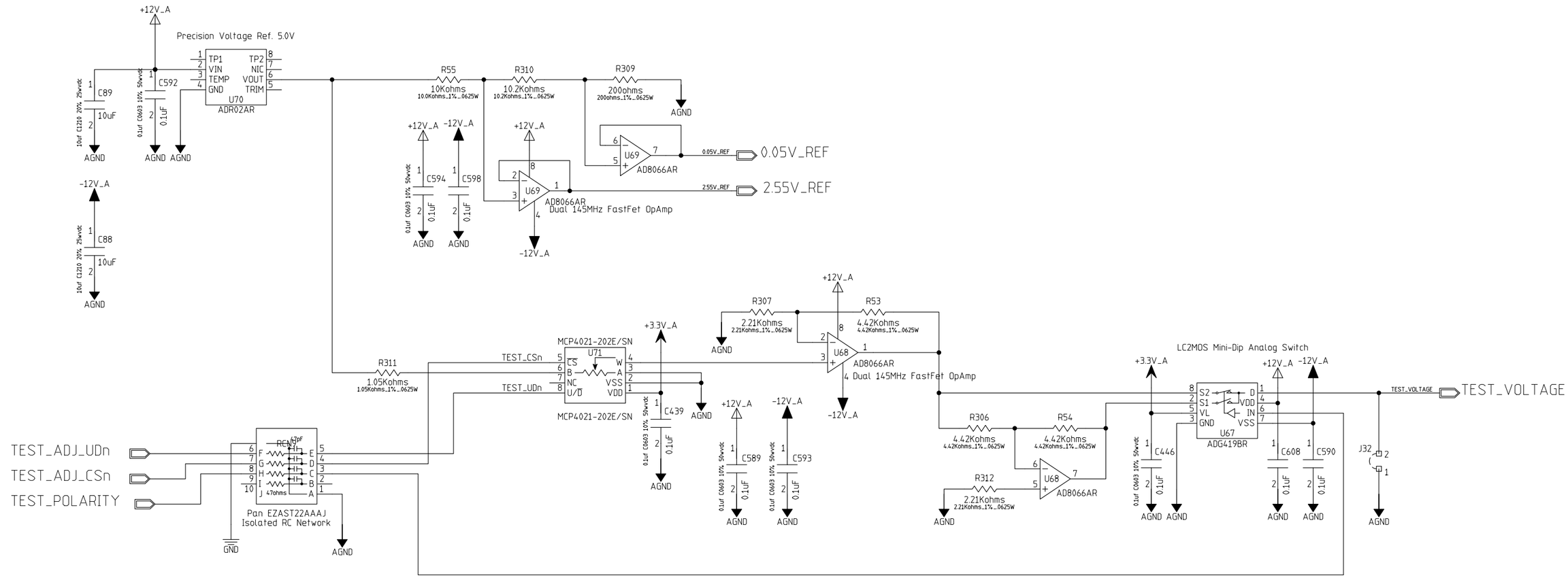

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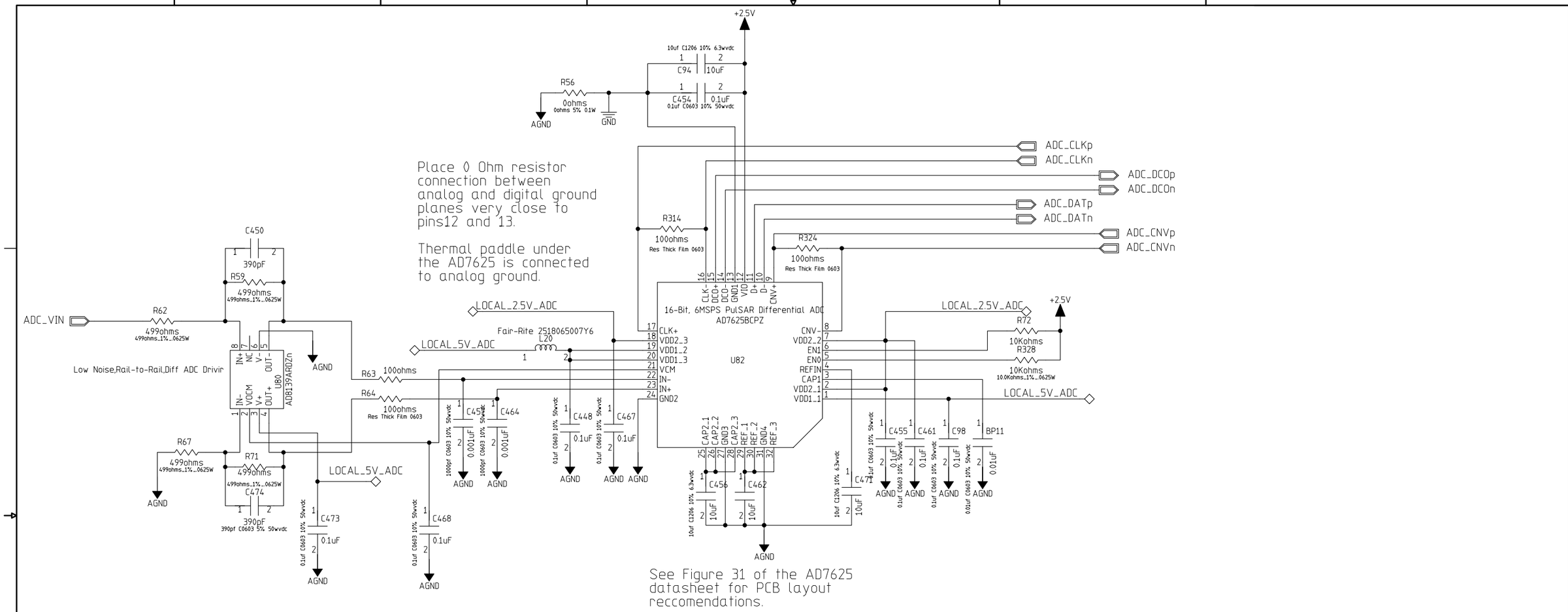

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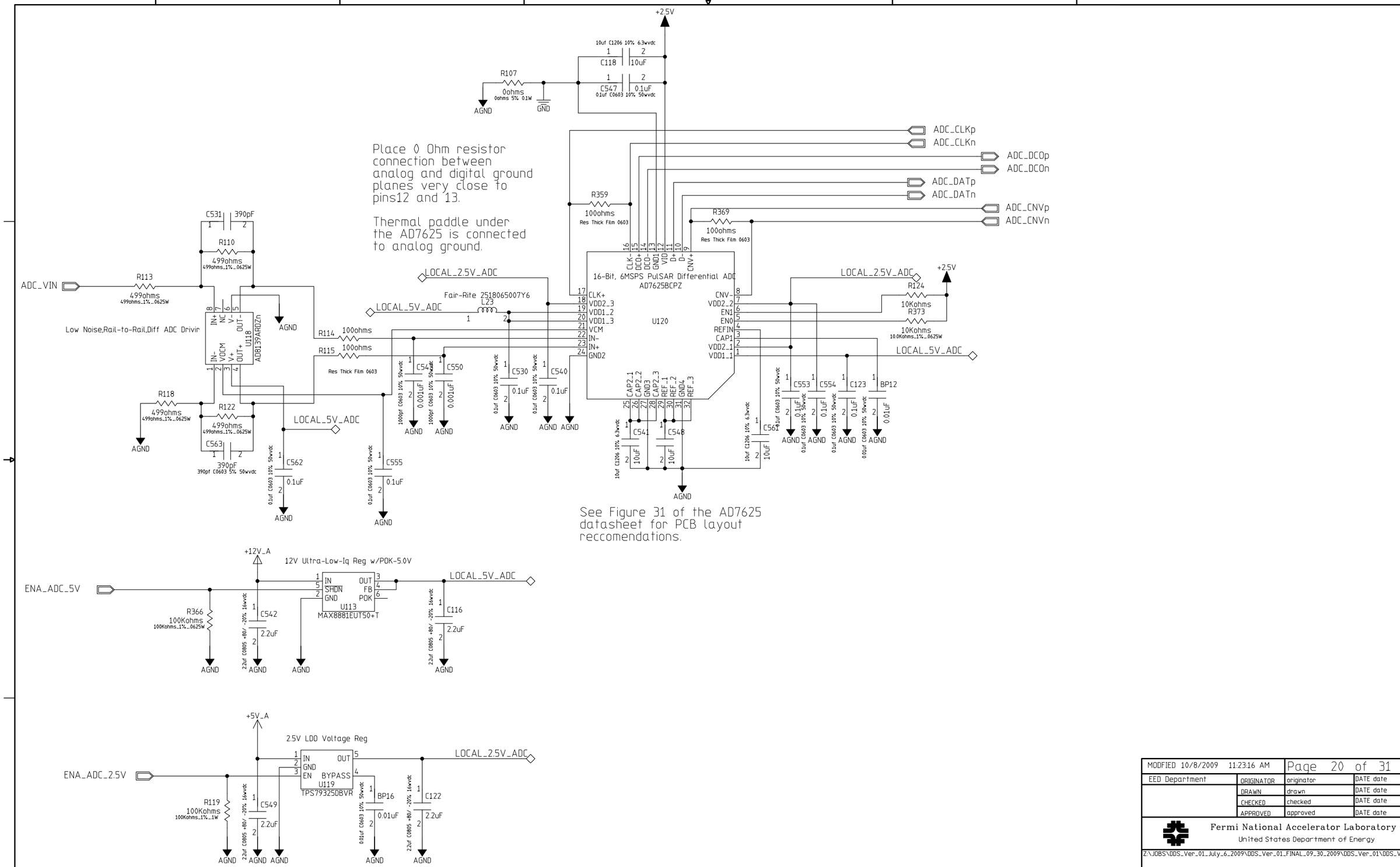

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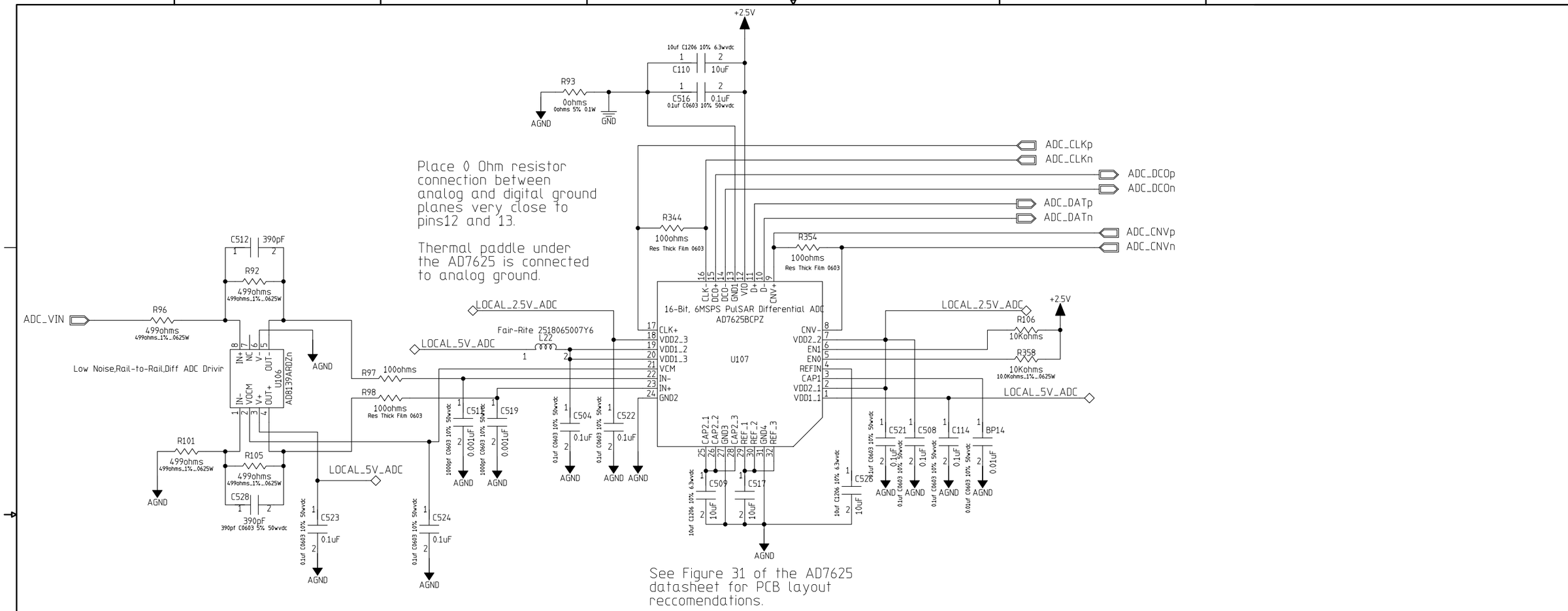

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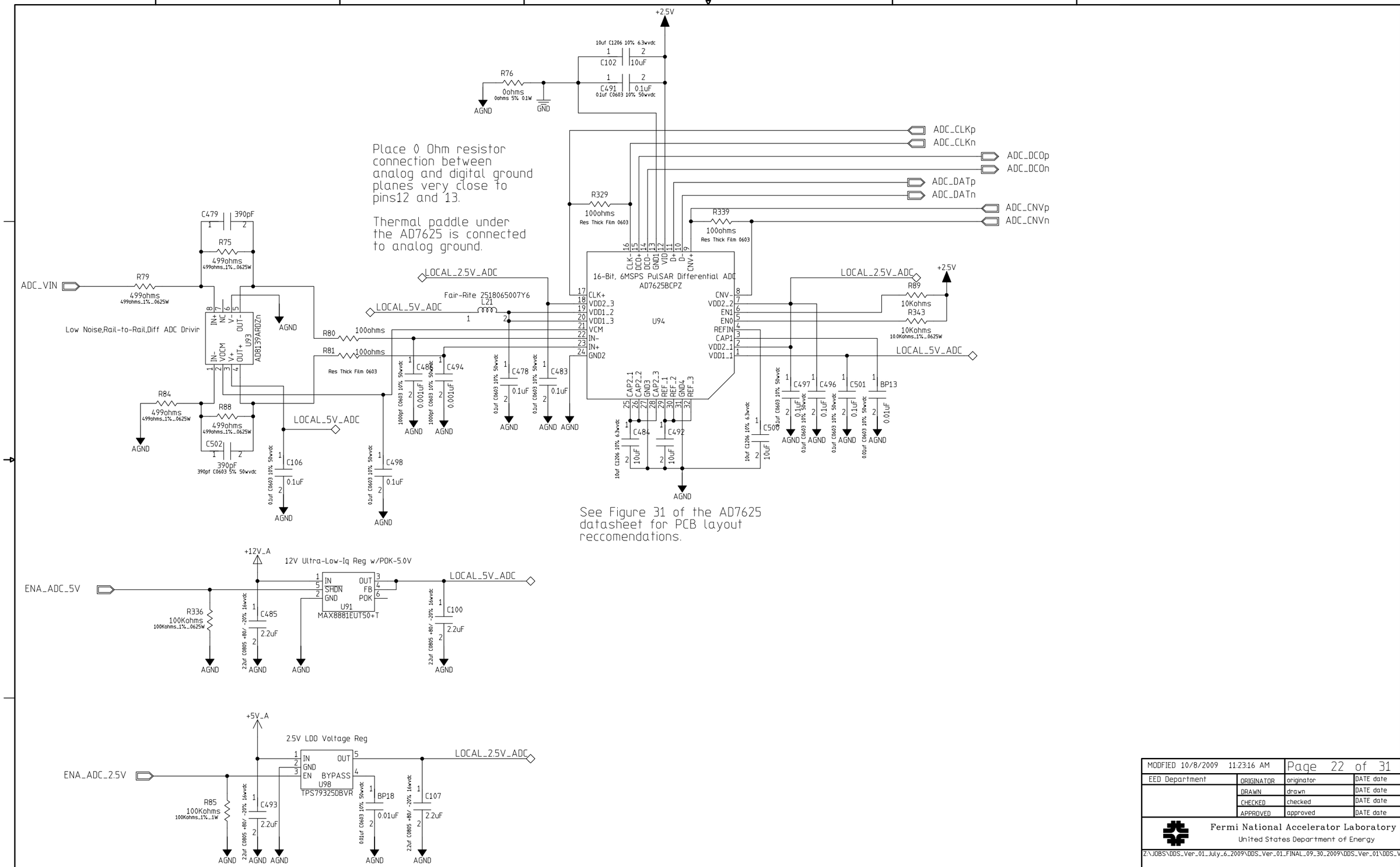

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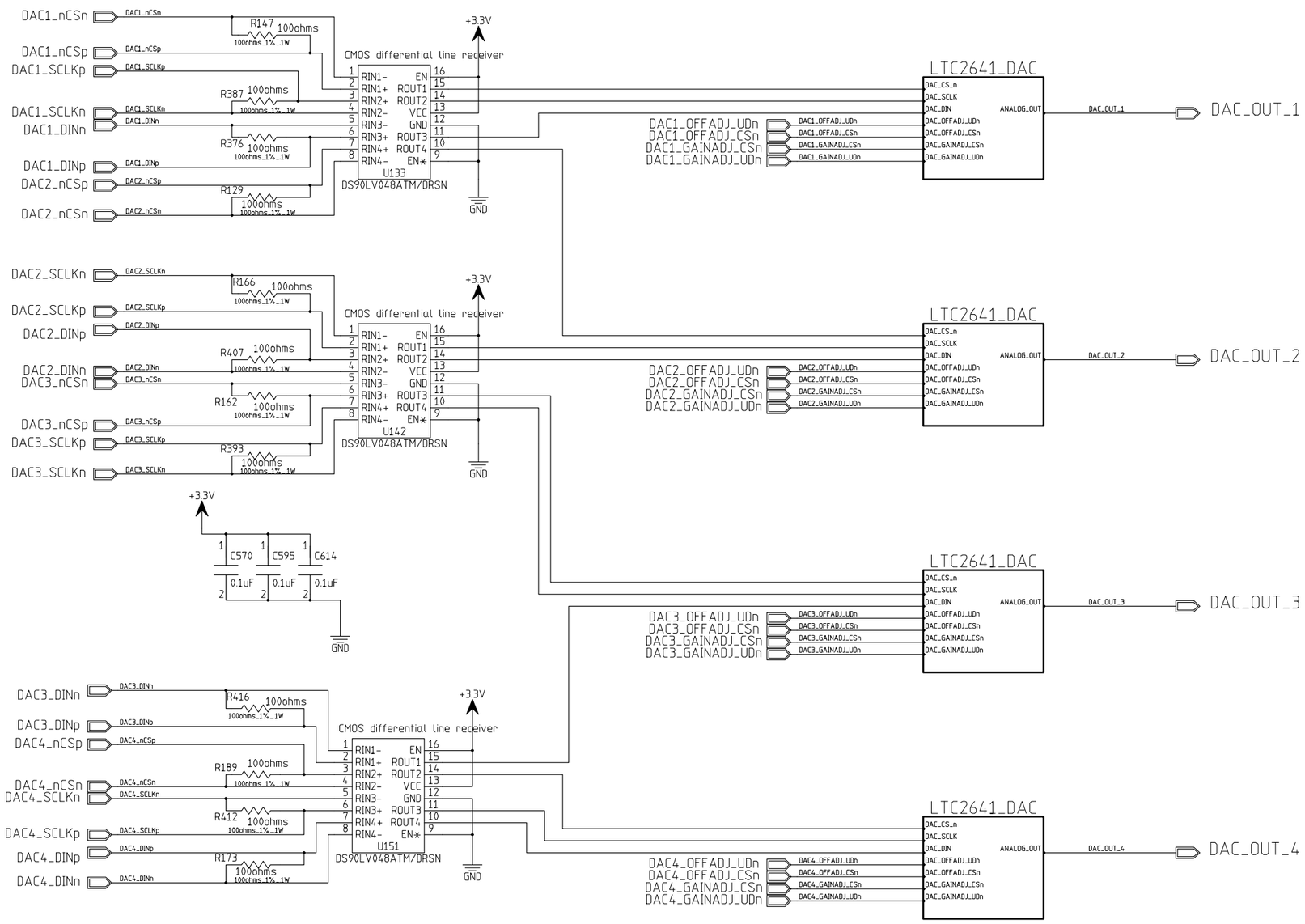

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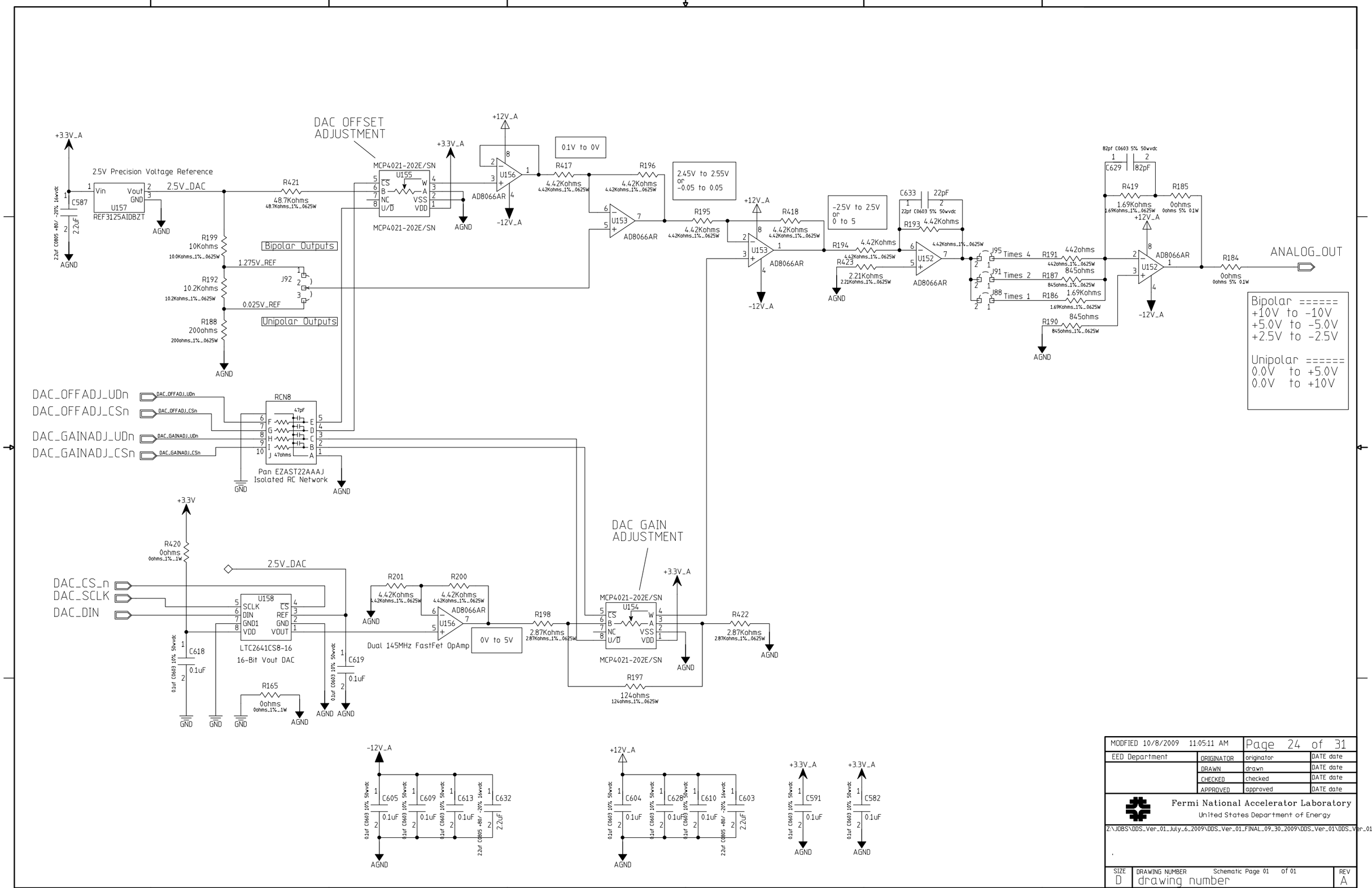

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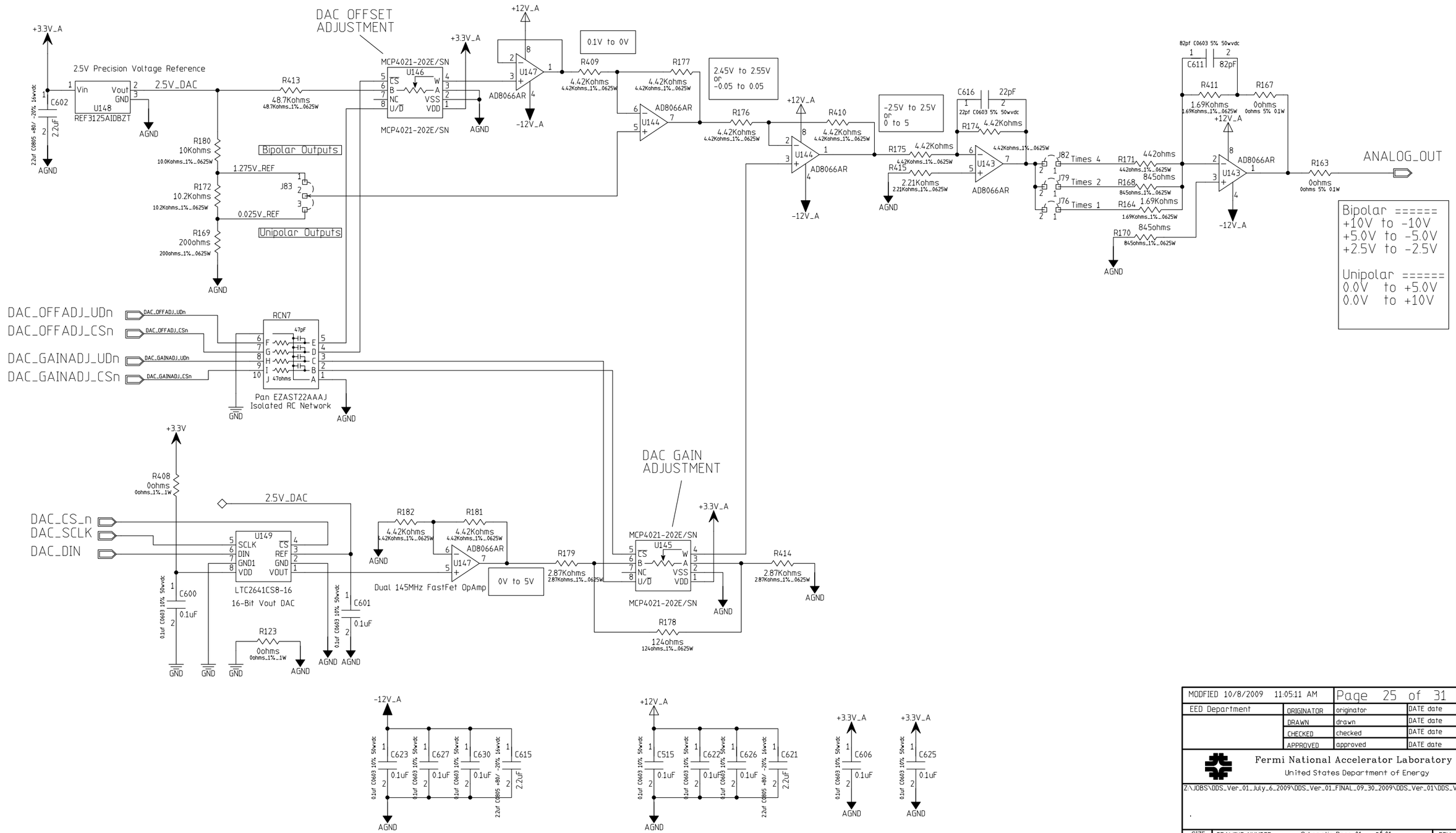

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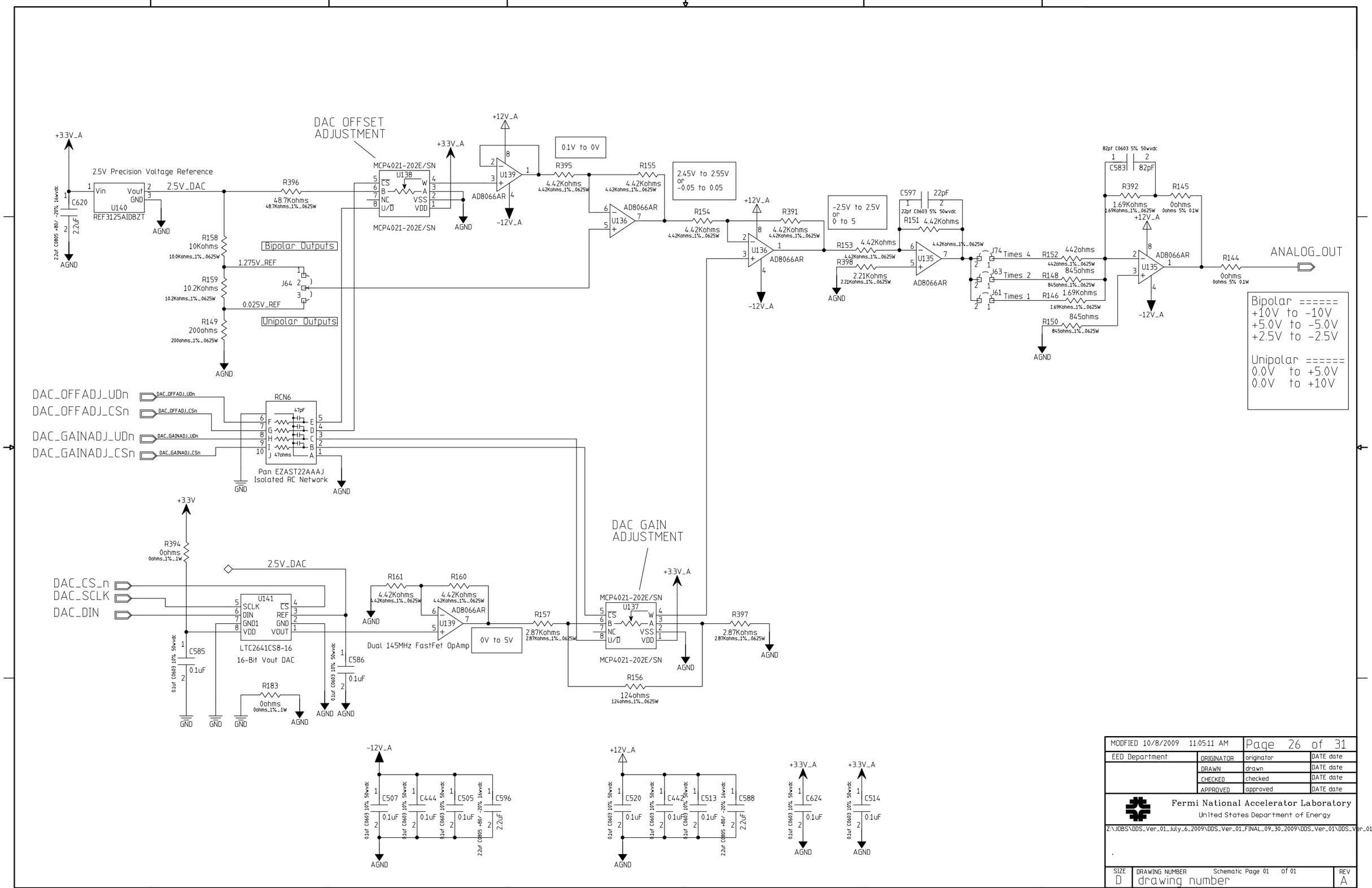

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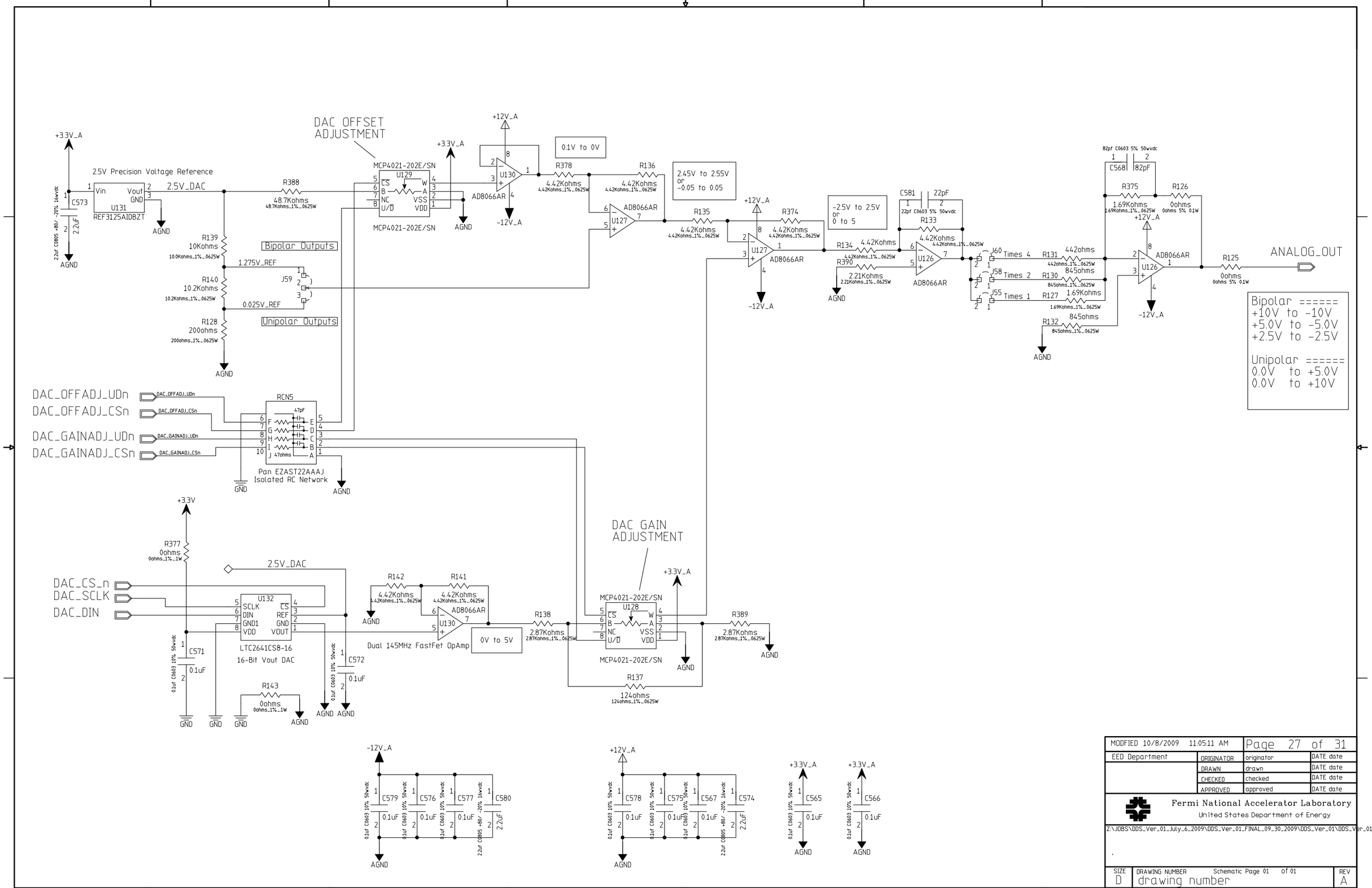

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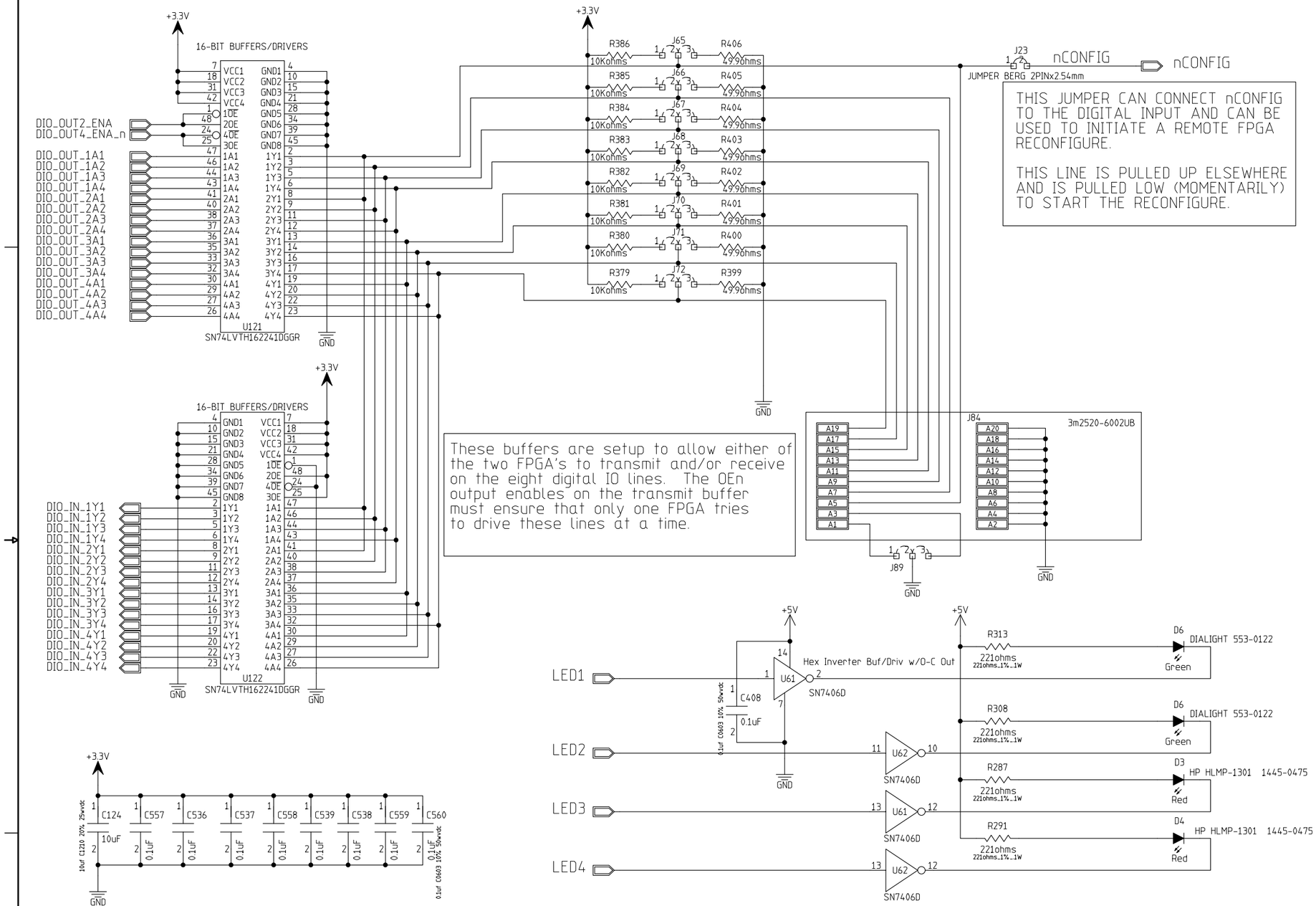

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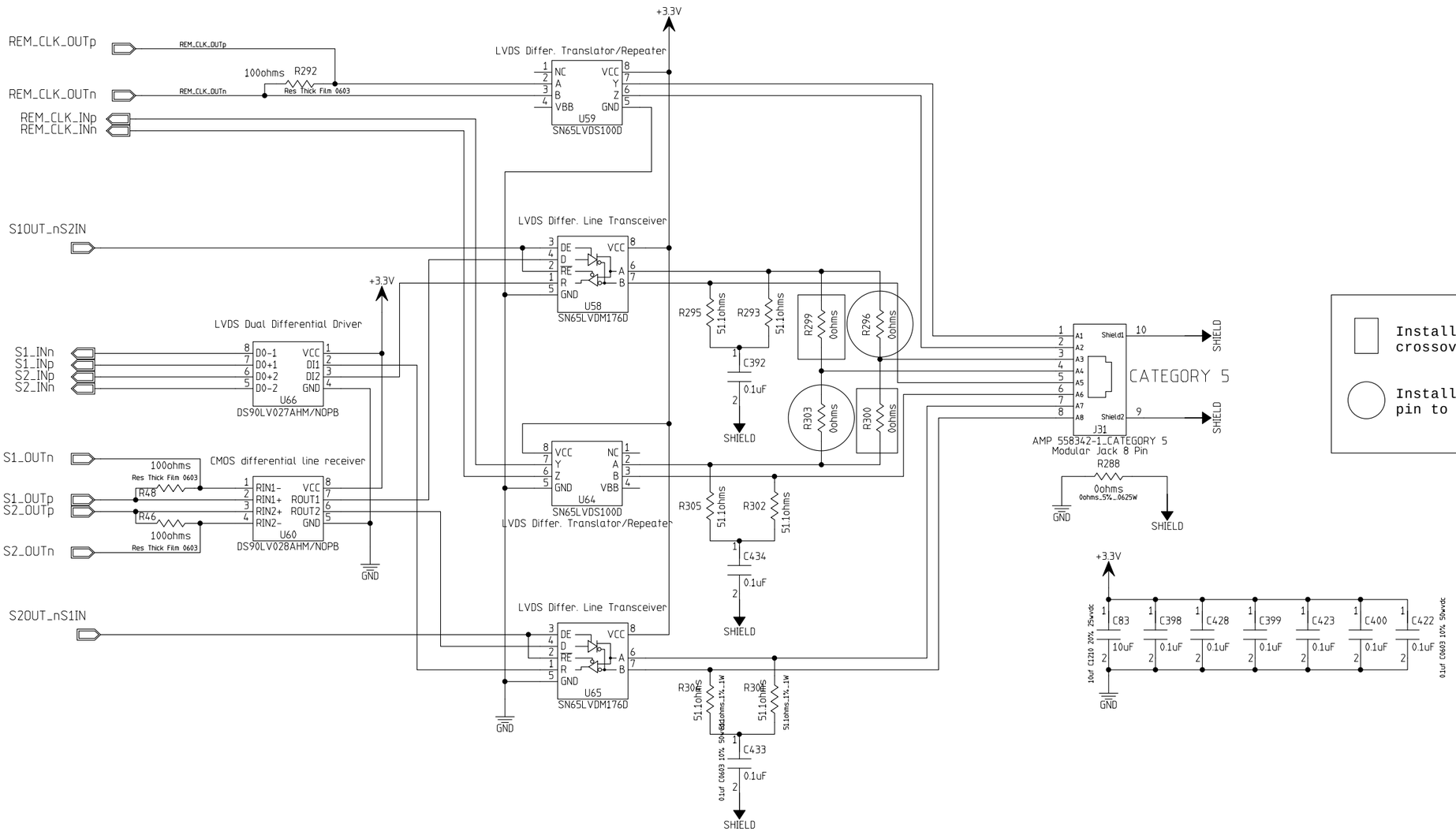

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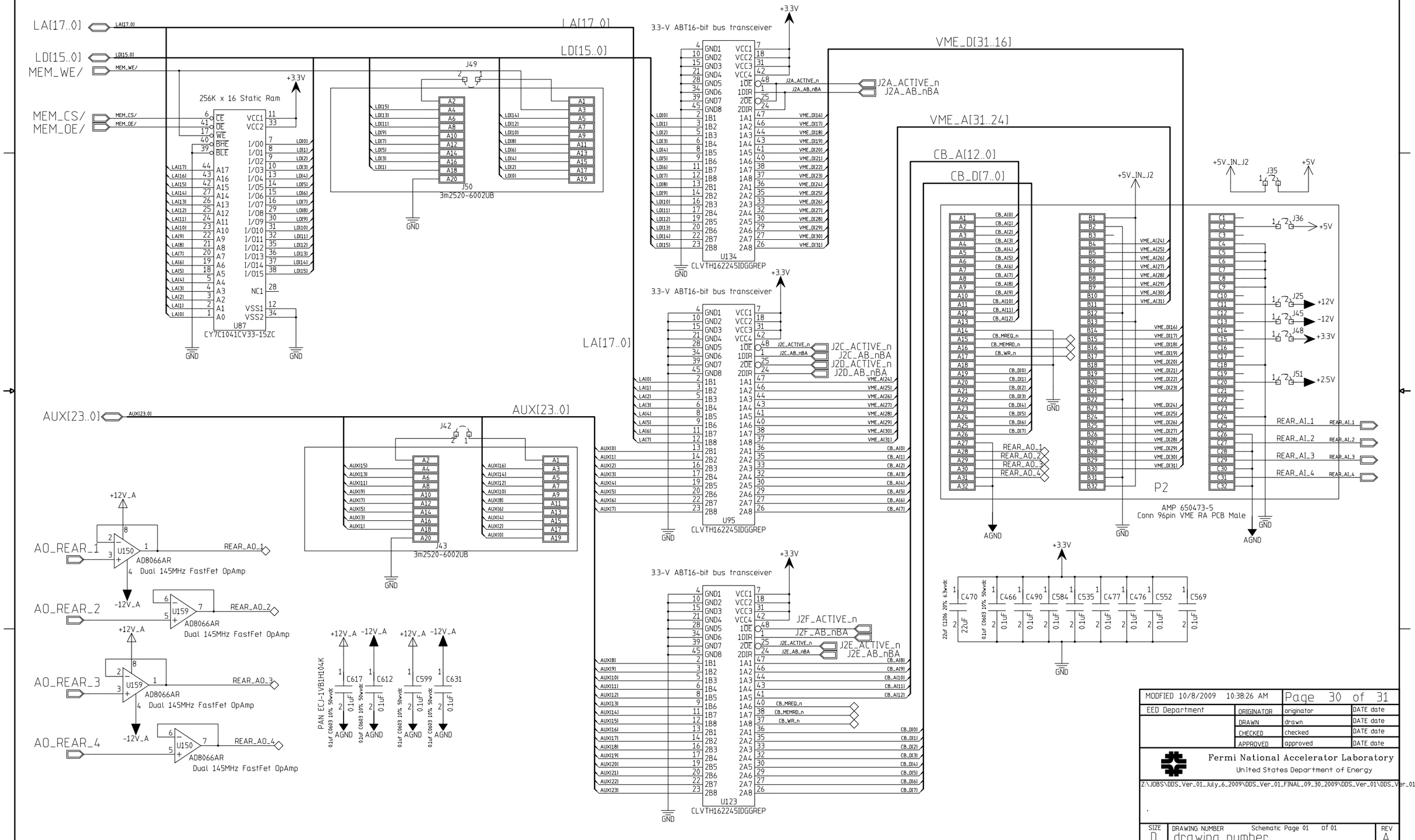

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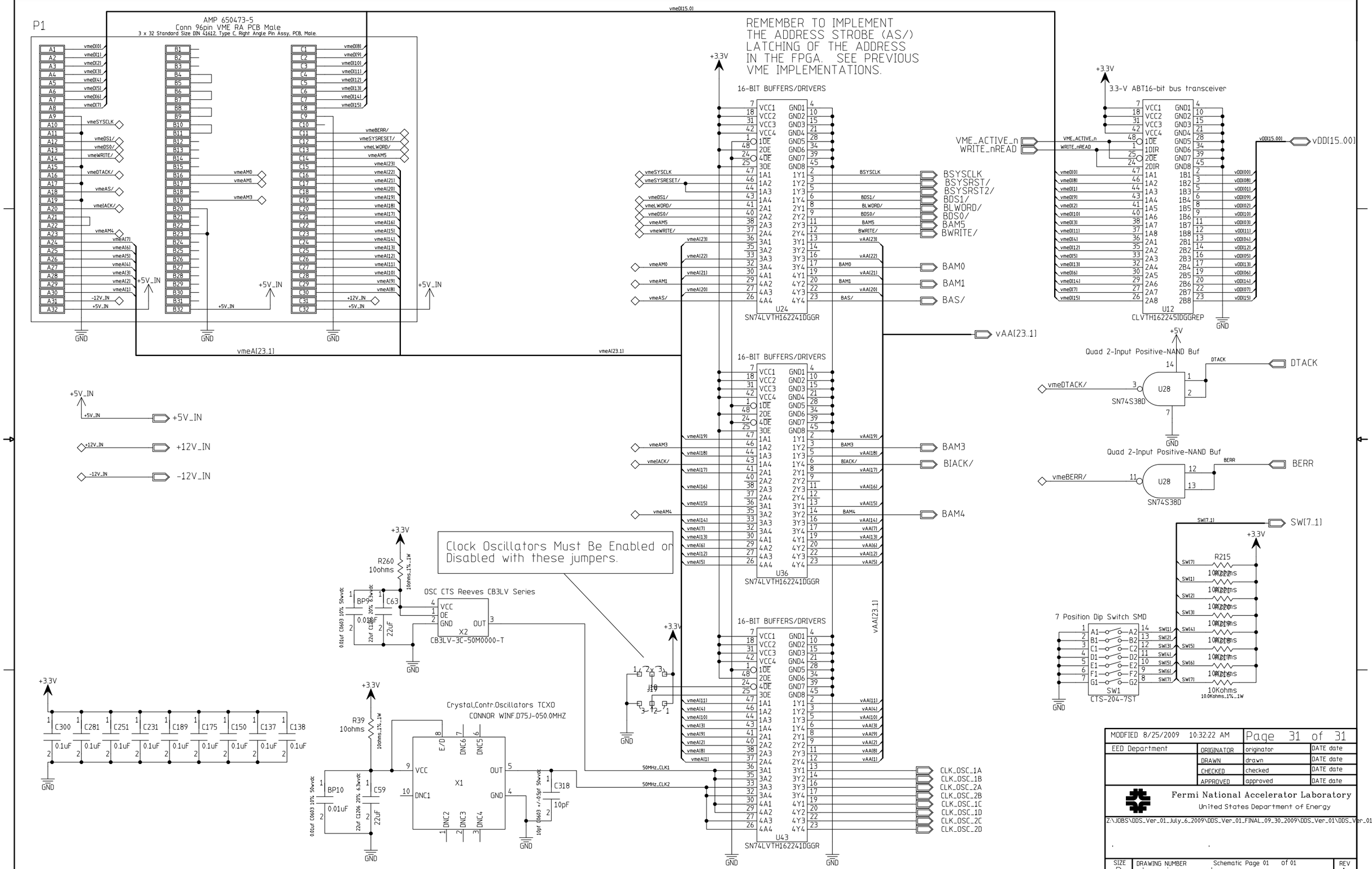
P1
AMP 650473-5
Conn 96pin VME RA PCB Male
3 x 32 Standard Size DIN 41612, Type C, Right Angle Pin Assy, PCB, Male.
REMEMBER TO IMPLEMENT THE ADDRESS STROBE (AS/) LATCHING OF THE ADDRESS IN THE FPGA. SEE PREVIOUS VME IMPLEMENTATIONS.
16-BIT BUFFERS/DRIVERS
U24
SN74LVTH162241DGGR
U36
SN74LVTH162241DGGR
U43
SN74LVTH162241DGGR
3.3-V ABT16-bit bus transceiver
U12
CLVTH162245DGGREP
Quad 2-Input Positive-NAND Buf
U28
SN74S38D
7 Position Dip Switch SMD
SW1
CTS-204-7ST
Clock Oscillators Must Be Enabled or Disabled with these jumpers.
OSC CTS Reeves CB3LV Series
X2
CB3LV-3C-50M0000-T
Crystal,Contr.Oscillators TCXO
CONNOR WINF.D75J-050.0MHZ
X1
J10
vme[23..1]
vme[15.0]
vAA[23..1]
vDD[15..00]
DTACK
BERR
SW[7..1]
BSYSCLK
BSYSRST/
BSYSRST2/
BDS1/
BLWORD/
BDS0/
BAM5
BWRITE/
BAM0
BAM1
BAS/
BAM3
BIACK/
BAM4
CLK_OSC_1A
CLK_OSC_1B
CLK_OSC_2A
CLK_OSC_2B
CLK_OSC_1C
CLK_OSC_1D
CLK_OSC_2C
CLK_OSC_2D
+5V_IN
+12V_IN
-12V_IN
+3.3V
+5V
GND
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