Fermi National Accelerator Laboratory

Tevatron/Main Injector BLM Upgrade Project
Abort Card Specification

Engineering Note

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1 INTRODUCTION

The Abort Cards are 6U by 160mm VME-based circuit boards that will be used to cause local abort signals based on abort information received from the Digitizer Cards via the proprietary "Control Bus". One Abort Card will reside in a dedicated "Abort System" VME crate along with other associated system cards. One such system will reside in each Main Ring or Main Injector Service building. The local abort signals will be cabled to the existing abort chassis in the building.. In addition, each card will be part of a serial link which sends abort information from house to house to a dedicated collection board located at A0. Functions and features are as follows:

- Reads the Abort information from each Digitizer Card once per revolution.
- Applies a channel mask and "multiplicity" requirement before requesting an abort .
- Stores the abort information in a VME-readable circular buffer for 65536 turns.
- Periodically sends this abort information to the next house, forming a serial data stream of abort information. Each successive house appends its data to the data stream.
- VME registers exist for reading the circular buffer, testing the memory, sending diagnostic signals, reading board ID information.
- Control Bus for setting the mask and multiplicity values, and for reading the Channel OK bits that were latched while reading abort information from the DCs.
- Abort bus for reading the abort bits from the Digitizer Cards.
- Masks and Multiplicity numbers are double-buffered..
- Front Panel Lemo outputs: Immediate Abort, Fast Abort, Slow Abort, Very Slow Abort.
- Front Panel BNCs: Abort Out, Serial Link In, and Serial Link Out..
- VME-originated diagnostic MakeMeas signal.
- VME Test of Serial Link
- VME interrupt capability to be specified.
- Front panel displays and LEDs show the board status.

2 I/O CONFIGURATION

2.1 General Crate Configuration

The Abort Cards (AC) will reside in a custom 6U by 160mm VME crate. Slot one in each crate will house a VME Master. The main purpose of the VMEBus is for diagnostics and to read the AC Board ID. The J1 backplane is a standard VME backplane. The custom J2 backplane will provide VME address lines A24 through A31 on column B. Columns A and C will provide the custom Control Bus and Abort Bus. Other cards in the crate will be the Controller Card (CC), The Timing Card (TC), up to fifteen Digitizer Cards (DC), and a High Voltage (HV) Card.

2.2 Interface to the Digitizer Cards (The Abort Bus)

The Abort Card is master of the Abort Bus, which is used to gather abort data for the crate. Upon receiving a Make Meas signal, the Abort Card sends addresses out on the AbortCS[5..0] and for each address sent it receives one channel's worth of abort data on the Abort[3..0] lines. These four bits correspond to the four "abort types" Immediate abort, Fast Abort, Slow Abort, Very Slow Abort (see system specification). If a bit is a "0" then the channel has a digitized value greater than its threshold value (preset in the Digitizer Card via the Control Bus). AbortCS[5..3] represent the DC board address, and AbortCS[1..0] represent the four individual channels per board. Upon receiving all the abort information, the Abort Card adds the number of channel hits per abort type and compares the value to a preset multiplicity value. Any value greater than the multiplicity sends an abort request to the Abort System via a BNC connector on the front panel. Each of the four abort types behaves independently in this manner, and four Lemo connectors exist on the front panel in case individual pulse information is desired. Each channel in the crate can also be "masked" to prevent its inclusion in an abort request. There are four masks per channel corresponding to the four abort types.

Abort 0	Immediate Abort
Abort 1	Fast Abort
Abort 2	Slow Abort
Abort 3	Very Slow Abort.

Table 1. The Abort lines on the Abort Bus and their relationship to the four abort types.

2.3 Control Bus Operations

The control bus is a simple bus for setting parameters. It consists of thirteen address lines, eight bidirectional data lines, and three control lines. It is a bus that operates without handshaking and relies on the slaves to respond within an allotted time.

The Abort Card uses the Control bus to set the abort mask bits (four per DC channel), and to set the 6-bit multiplicity value for each of the four abort types. The bus is also used for a "force abort" function. The "Channel Okay" register reflects the status of the backplane's CH OK line during the read of the abort status of each channel. These bits are latched and written into the four LSBs of each byte, so there is one byte per card. The latches are reset by the "Reset DC" line on the backplane. The Abort Card's Control Bus registers are as follows.

Masks:		Address(A7-A0) 00-FF
1[6]	Abort MaskR/W	00
1[6]	Abort Channel Count	01
8[64]	Immediate Abort Masks R/W	10-17
8[64]	Fast Abort Masks R/W	18-1F
8[64]	Slow Abort Masks R/W	20-27
8[64]	Very Slow Abort Masks R/W	28-2F
Multiplicities:		
1[6]	Immediate Multiplicity R/W	40
1[6]	Fast Multiplicity R/W	41
1[6]	Slow Multiplicity R/W	42
1[6]	Very Slow Multiplicity R/W	43
General:		
1[6]	Force Abort H R/W	45
1[6]	Force Abort L R/W A4	
1[6]	Force Abort Permit R/W	A5
1[4]	Interrupt Register R/W	A6
Diagnostic:		
2[16]	ADC Temperature R	4E-4F
16[64]	Channel Okay R	50-5F

Table 2. Control Bus Registers in the Abort Card

Control Bus Interrupt Register data format (R/W):

D07	Zero
D06	Zero
D05	Zero
D04	Clear IRQ3
D03	Zero
D02	Assert IRQ3 when an abort occurs before multiplicity is applied
D01	Assert IRQ3 when any Channel "not OK"
D00	Assert IRQ3 when an abort occurs

2.4 VMEbus Operations

The VME portion of the AC is an A32/D16 Slave. Functions are:

- To provide Board ID and other general information
- Control/Status register for diagnostic control
- Reading of the circular buffer of abort history information
- Testing of this circular buffer memory
- Testing of the Inter-House Serial Link

2.4.1 VMEbus Address Map (A32/D16 Slave)

A31-A24	A23 – A00	Description
30	000000-000FFE	8kB of Settings, ID etc.
30	020000	Interrupt Register
30	030000	Abort Status Register
30	040000-040002	Memory Pointer
30	050000	Memory Test Register
30	050010	Serial Diagnostic Register
30	050020	Abort Test Register
30	060000	Serial Link Test
30	070000	Position in Serial data stream
30	200000-3FFFFE	Abort History Circular Buffer

Table 3. VME Registers

AIP (Abort in Progress) must be active to enable VME reads of the Circular Buffer.

2.4.2 VME Register Data Formats

Interrupt Register data format:

D15 – D08	Zeroes
D07	Zero
D06	Zero
D05	Zero
D04	Clear IRQ3
D03	Serial Link Error
D02	Assert IRQ3 when an abort occurs before multiplicity is applied
D01	Assert IRQ3 when any Channel “not OK”
D00	Assert IRQ3 when an abort occurs

Note: The states of Address lines A01-A03, and the Status/ID returned during an interrupt service routine shall be agreed-upon by the software designer and the author.

Abort Status Register data format:

D15 – D08	Zeroes
D07	AIP
D06	Zero
D05	Very Slow Abort
D04	Slow Abort
D03	Fast Abort
D02	Immediate Abort
D01	Zero
D00	Running

Memory Pointer Register data format (R):

D03 – D00	Memory address bits A19 – A16	040002
D15 – D00	Memory address bits A15 – A00	040000

Memory Test Register data format (R/W):

D15 – D08	Zeroes
D07	Zero
D06	Zero
D05	Zero
D04	Reset Memory Pointer
D03	Zero
D02	Zero
D01	Zero
D00	Memory Test Mode

Serial Diagnostic Register data format (R/W):

D15 – D08	Zeroes
D07	Zero
D06	Zero
D05	Zero
D04	Serial Link Test mode
D03	Zero
D02	Zero
D01	Zero
D00	Serial Link Test Begin

Abort Test Register data format (R/W):

D15 – D08	Zeroes
D07	Zero
D06	Zero
D05	Zero
D04	Send Diagnostic MakeMeas signal
D03	Zero
D02	Zero
D01	Zero
D00	Reset Logic

Serial Link Test Register data format (R/W)::

D15 – D00	Write 16 words here, then assert “Begin”

Serial Position Register data format (R/W):

D04 – D00	Assigns house number 1 to 30

Abort History data format:

Each table entry has four bits representing each of the four abort types (except for the last two rows), therefore each row represents a VME WORD read.) The bits are derived directly from the Digitizer Card before the abort masks are applied. When writing the addresses are decremented, so upon reading, the VME Master should increment the address by 20 hex for each turn back in time.

Board 1, Channel 4	Board 1, Channel 3	Board 1, Channel 2	Board 1, Channel 1
Board 2, Channel 4	Board 2, Channel 3	Board 2, Channel 2	Board 2, Channel 1
Board 3, Channel 4	Board 3, Channel 3	Board 3, Channel 2	Board 3, Channel 1
Board 4, Channel 4	Board 4, Channel 3	Board 4, Channel 2	Board 4, Channel 1
Board 5, Channel 4	Board 5, Channel 3	Board 5, Channel 2	Board 5, Channel 1
Board 6, Channel 4	Board 6, Channel 3	Board 6, Channel 2	Board 6, Channel 1
Board 7, Channel 4	Board 7, Channel 3	Board 7, Channel 2	Board 7, Channel 1
Board 8, Channel 4	Board 8, Channel 3	Board 8, Channel 2	Board 8, Channel 1
Board 9, Channel 4	Board 9, Channel 3	Board 9, Channel 2	Board 9, Channel 1
Board 10, Channel 4	Board 10, Channel 3	Board 10, Channel 2	Board 10, Channel 1
Board 11, Channel 4	Board 11, Channel 3	Board 11, Channel 2	Board 11, Channel 1
Board 12, Channel 4	Board 12, Channel 3	Board 12, Channel 2	Board 12, Channel 1
Board 13, Channel 4	Board 13, Channel 3	Board 13, Channel 2	Board 13, Channel 1
Board 14, Channel 4	Board 14, Channel 3	Board 14, Channel 2	Board 14, Channel 1
F A S T A B O	R T | I M M	E D. A B O R T	Four crate aborts
S L O W A B O	R T | V. S L	O W A B O R T	Not Defined

Table 4. Data format of one house's worth of abort data. There will be 64K of these "tables" stored consecutively in the circular buffer.

2.5 Inter-House Serial Link

The Serial Link will transmit the information shown in Table 4 for each house via a high quality copper coaxial cable to a specially-configured Abort Card located near A0 which will serve as the collection point and processing center of the information. Each house will receive the previous house's information and rebroadcast it onto the cable, adding its information to the end of the data stream. Each house will have a register for assigning its position in the data stream so it will know when to append its data. A0 will send a "preamble" to House A1 which will recognize this and put its 256 bits into the stream. The next house will receive this bitstream and will place its 256 bits at the end of the data stream. When the bitstream returns to A0 via F4, there will be a preamble and 30 houses worth of data.

The serial link utilizes the Cypress HotLink transceiver operating at 60 Mbaud. Because of the cable lengths involved between houses, an adaptive equalizer chip compensates for the loss of high-frequency components of the signal caused by skin effect.

At 60 Mbaud, the fastest all the information can traverst the ring is 160μs:
256 bits per house x 30 houses = 7680 bits
7680 x (10/8) = 9600 bits ; 9600 bits x 16.7ns/bit = 160μs.

AC Block Diagram

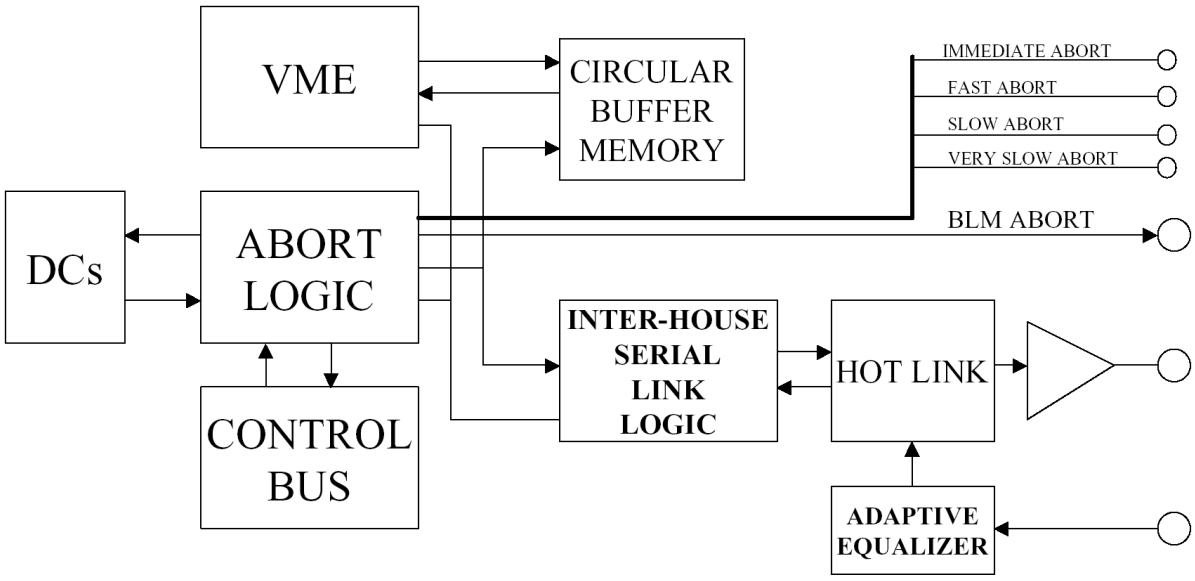

Figure 1. Block Diagram of Abort Card