Data Transfer Protocol for the USB to FIFO Interface

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Introduction

This document describes the protocol for transferring data between the LLRF DDS-VME Module and a PC computer using the FTDI Chip UM245R USB-Parallel FIFO Development Module. This is a small module that is plugged into our circuit as a daughter board. There are 8 bidirectional data lines, a transmitter buffer empty (TXE) signal, a receiver full (RXF) signal and read / write control signals for interfacing the USB module to our circuit.

The data on our LLRF DDS-VME Module is typically 32 bit and sometimes 16 bit. Therefore, we need a simple protocol for reading and writing this data through the 8 bit wide data bus of the USB module. In addition to addressing the data one word at a time, we will also want to define some faster transfer modes to upload or download larger blocks of data, and we may wish to implement some control commands that the PC could issue to the DDS module.

**Currently the protocol does not provide for acknowledgement messages sent between the DDS Module and the PC. This is being considered. A "Ready" response (0xA5) is defined for Writes to the DDS Module since memory access in the module may be held off, at times, by other processes. During Read operations the PC knows things are proceeding when it starts receiving data. During commands we may want to send an acknowledgement. For Single Channel Reads and Writes the DDS Module is expected to implement dedicated registers that data can be read or written quickly.*

The Structure

The PC will be the master of all of the data transfers. The tables below layout bits for 8 transfer modes (3 bits), 2,097,152 ***byte*** addresses (21 bits) and a transfer ***byte*** count up to 65,536. The Full Address Mode for transferring blocks of data is to set the starting address using the first three bytes transmitted to the DDS module, and then send the number of data words to transfer in the next two bytes. The address pointer in the DDS module is expected to increment from the starting address. Note the address is the byte address in the DDS Module memory map. Here a byte is 8 bits. Hence, a single transaction can access up to 65,536/4 = 16,384, 32 bit words.

The three mode bits, along with the 5 address bits in the first header byte, allow us to define control commands and single data word accesses that require only this single header byte be transmitted.

Address Mode	MODE			ADDR[20 ... 16]				
Bit	7	6	5	4	3	2	1	0
Full Address Mode, Read	0	0	0	A20	A19	A18	A17	A16
Full Address Mode, Write	0	0	1	A20	A19	A18	A17	A16
Single Channel Mode, Read	0	1	0	Ch4	Ch3	Ch2	Ch1	Ch0
Single Channel Mode, Write	0	1	1	Ch4	Ch3	Ch2	Ch1	Ch0
Command Mode	1	0	0	Cmd4	Cmd3	Cmd2	Cmd1	Cmd0
reserved	1	0	1	x	x	x	x	x
reserved	1	1	0	x	x	x	x	x
Reset Interface	1	1	1	x	x	x	x	x

Address Mode	Description
Full Address Mode, Read [000]	All five bytes of the Data Transfer Header are sent. This is the full 21 bit address and 16 bit byte count. After the header is received by the DDS Module, the DDS Module will transmit the requested data through the USB module.
Full Address Mode, Write [001]	All five bytes of the Data Transfer Header are sent. After the header is received the DDS Module will transmit the Ready response (0xA5) to the PC. The PC will then transmit to the DDS Module the number of bytes given in the header.
Single Channel Mode, Read [010]	A single header byte is transmitted with the Ch[4..0] bits addressing a dedicated register in the DDS Module. The reception of this header byte is followed by the DDS Module transmitting the data in the addressed register.
Single Channel Mode, Write [011]	A single header byte is transmitted with the Ch[4..0] bits addressing a dedicated register in the DDS Module. The transmission of data bytes from the PC to the addressed DDS Module follows immediately.
Command Mode [100]	A single header byte is transmitted with the Cmd[4..0] bits set to signal a specific control command, such as start, stop, reset a process, etc..
reserved	Not yet defined.
Reset Interface	Resets the protocol state machine and can terminate transfers in process.

Data Transfer Header

Address Mode / Address 1	MODE			ADDR[20 ... 16]				
	7	6	5	4	3	2	1	0
Address 2	ADDR[15 ... 8]							
	7	6	5	4	3	2	1	0
Address 3	ADDR[7 ... 0]							
	7	6	5	4	3	2	1	0
Byte Count 1	COUNT[15 ... 8]							
	7	6	5	4	3	2	1	0
Byte Count 2	COUNT[7 ... 0]							
	7	6	5	4	3	2	1	0

Data Transfer Order

Data Word [0]	Byte 0 (LSB)							
	7	6	5	4	3	2	1	0
	Byte 1							
	7	6	5	4	3	2	1	0
	Byte 2							
	7	6	5	4	3	2	1	0
	Byte 3 (MSB)							
	7	6	5	4	3	2	1	0

Data Word [1]	Byte 0 (LSB)							
	7	6	5	4	3	2	1	0
	Byte 1							
	7	6	5	4	3	2	1	0
	Byte 2							
	7	6	5	4	3	2	1	0
	Byte 3 (MSB)							
	7	6	5	4	3	2	1	0

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Data Word [N]	Byte 0 (LSB)							
	7	6	5	4	3	2	1	0
	Byte 1							
	7	6	5	4	3	2	1	0
	Byte 2							
	7	6	5	4	3	2	1	0
	Byte 3 (MSB)							
	7	6	5	4	3	2	1	0