Users Guide for the Dual Phase Detector Module

For Booster Acceleration and MI Phase Lock Control

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Version 2

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I. Introduction

The Dual Phase Detector Module is a NIM module providing two AD8302 phase detectors, two ADC converters, three DAC analog outputs, 8 digital inputs and 8 each 50 Ohm digital outputs all tied together with an Altera Cyclone FPGA. The module also includes 64kx16 SRAM memory, Flash memory for parameter storage, a USB PC interface with PC Windows interface software and an Ethernet port that we have hopes of writing the firmware for in the near future.

The Dual Phase Detector Module has many features that make it flexible and hence potentially complicated for the user. Implemented within the FPGA are registers for setting gain, offsets and other parameters. The Non-volatile Flash memory is used on the module to retain settings once they are made.

The primary application for this module is to be able to provide the phase error feedback and control used to perform the Booster acceleration phase lock and the Main Injector phase lock functions. In doing this, this module could eventually replace the following LLRF NIM modules:

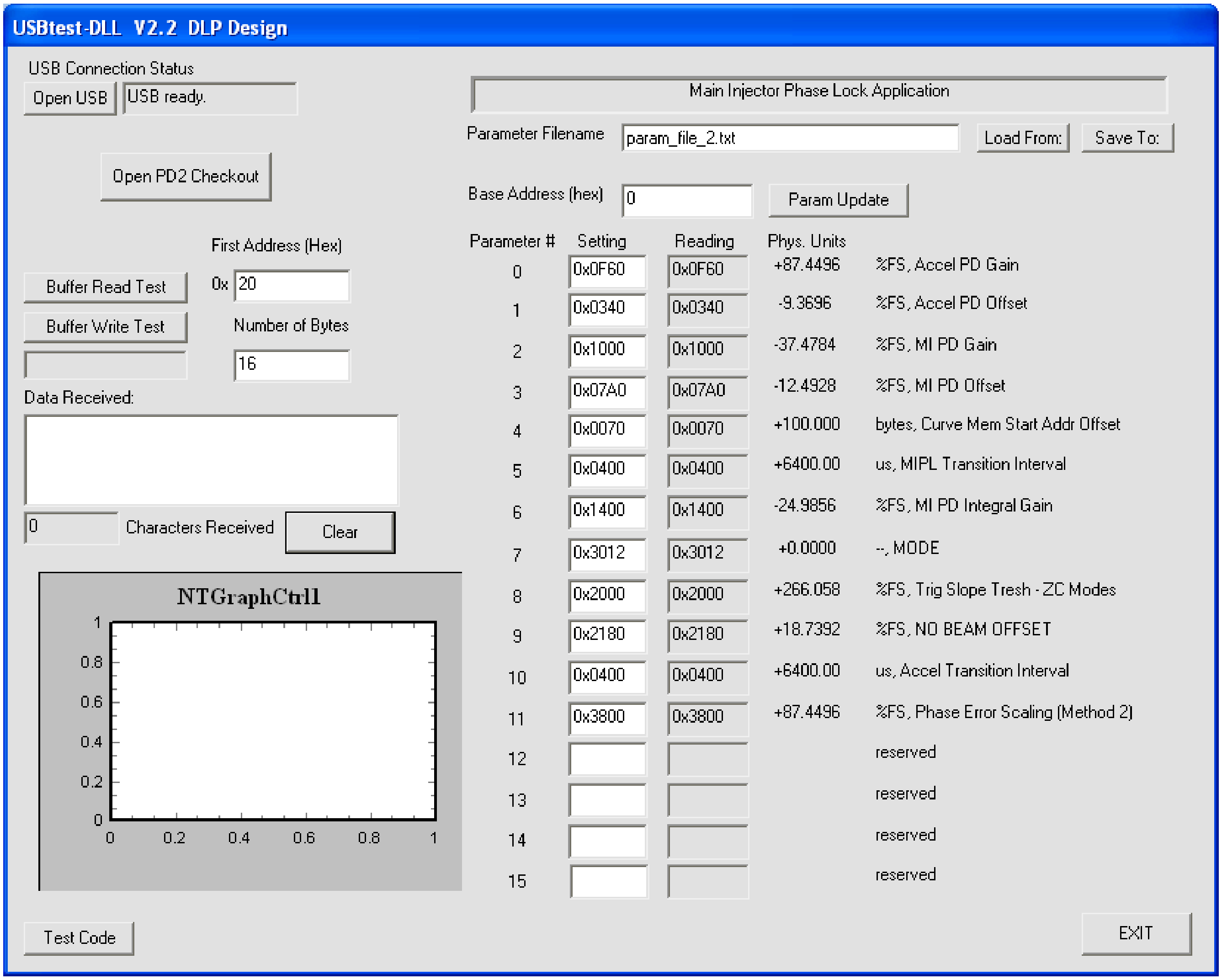
1. The Timing Generator, 0331.00-ED-180859
2. The 32 Countdown Module, 0331.00-EC-180846
3. The High Stability EMI Protected Phase Detector
4. The Program Generator, 0331.00-ED-180850
5. The Parabola Zero Box, 0331.00-EC-180858
6. The Fast Phase Detector, 0331.00-ED-180843
7. The Mode Controller, 0331.00-ED-180845

There are currently six Dual Phase Detector Modules that have been assembled. Opportunities for testing these modules with the rest of the LLRF system and with Booster beam are rare, but some progress has been made.

II. USB Interface

In order to program and examine the various registers on the module a USB interface has been implemented. The Dual Phase Detector uses a USB to 8 bit FIFO interface chip from FTDI, the UM245R. Drivers and documentation for this device are available from www.ftdichip.com, and also archived with this document. A simple data transfer protocol has been establish and specified in the document “Data Transfer Protocol for the USB to FIFO Interface”, also available in the DocDB or otherwise archived with this document. Both the firmware, FPGA processes on the module that manage the data transfer with the USB and the Windows PC software interface abide by this protocol.

Currently, the PC interface program is called USBtest.exe. Screen shots of the current version are shown below. The first screen has been used with the development and testing of the MI phase lock application. The second screen was created to aid in the checkout of the production testing of the modules.



USBtest-DLL V2.2 DLP Design

USB Connection Status: USB ready.

First Address (Hex): 0x 20

Number of Bytes: 16

Data Received:

0 Characters Received

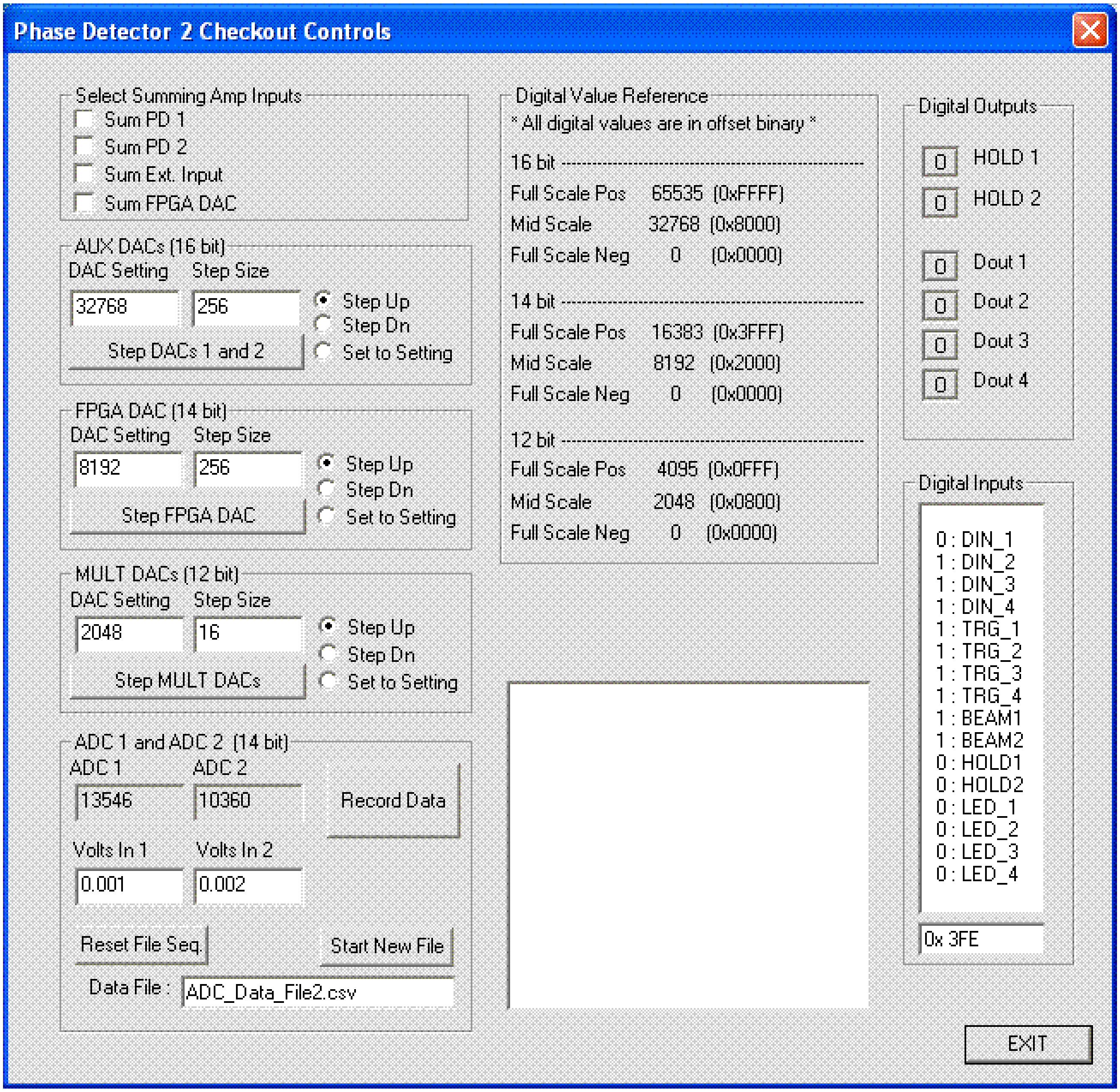
Main Injector Phase Lock Application

Parameter Filename: param_file_2.txt

Base Address (hex): 0

Parameter #	Setting	Reading	Phys. Units	
0	0x0F60	0x0F60	+87.4496	%FS, Accel PD Gain
1	0x0340	0x0340	-9.3696	%FS, Accel PD Offset
2	0x1000	0x1000	-37.4784	%FS, MI PD Gain
3	0x07A0	0x07A0	-12.4928	%FS, MI PD Offset
4	0x0070	0x0070	+100.000	bytes, Curve Mem Start Addr Offset
5	0x0400	0x0400	+6400.00	us, MIPL Transition Interval
6	0x1400	0x1400	-24.9856	%FS, MI PD Integral Gain
7	0x3012	0x3012	+0.0000	--, MODE
8	0x2000	0x2000	+266.058	%FS, Trig Slope Tresh - ZC Modes
9	0x2180	0x2180	+18.7392	%FS, NO BEAM OFFSET
10	0x0400	0x0400	+6400.00	us, Accel Transition Interval
11	0x3800	0x3800	+87.4496	%FS, Phase Error Scaling (Method 2)
12				reserved
13				reserved
14				reserved
15				reserved

Figure II.1 Initial dialog control for the Dual Phase Detector Module interface program.



Phase Detector 2 Checkout Controls

Select Summing Amp Inputs

- □ Sum PD 1
- □ Sum PD 2
- □ Sum Ext. Input
- □ Sum FPGA DAC

AUX DACs (16 bit)

DAC Setting	Step Size	
32768	256	● Step Up ○ Step Dn ○ Set to Setting

Step DACs 1 and 2

FPGA DAC (14 bit)

DAC Setting	Step Size	
8192	256	● Step Up ○ Step Dn ○ Set to Setting

Step FPGA DAC

MULT DACs (12 bit)

DAC Setting	Step Size	
2048	16	● Step Up ○ Step Dn ○ Set to Setting

Step MULT DACs

ADC 1 and ADC 2 (14 bit)

ADC 1	ADC 2
13546	10360

Record Data

Volts In 1	Volts In 2
0.001	0.002

Reset File Seq. Start New File

Data File : ADC_Data_File2.csv

Digital Value Reference

* All digital values are in offset binary *

16 bit		
Full Scale Pos	65535	(0xFFFF)
Mid Scale	32768	(0x8000)
Full Scale Neg	0	(0x0000)
14 bit		
Full Scale Pos	16383	(0x3FFF)
Mid Scale	8192	(0x2000)
Full Scale Neg	0	(0x0000)
12 bit		
Full Scale Pos	4095	(0x0FFF)
Mid Scale	2048	(0x0800)
Full Scale Neg	0	(0x0000)

Digital Outputs

0	HOLD 1
0	HOLD 2
0	Dout 1
0	Dout 2
0	Dout 3
0	Dout 4

Digital Inputs

```
0 : DIN_1
1 : DIN_2
1 : DIN_3
1 : DIN_4
1 : TRG_1
1 : TRG_2
1 : TRG_3
1 : TRG_4
1 : BEAM1
1 : BEAM2
0 : HOLD1
0 : HOLD2
0 : LED_1
0 : LED_2
0 : LED_3
0 : LED_4
```

0x 3FE

Figure II.2 Module production checkout dialog control.

For the MI phase lock application we have 12 parameter registers that are used. The definition of these parameters is given in Table II.1. These parameter register on the module may have alternate uses under the production checkout context.

Table II.1 Parameters defined for the MI Phase Lock application.

<table>
<tr><th>Register Name</th><th>Parameter Number</th><th>Data Format</th><th>Description</th></tr>
<tr><td>Channel A Gain
(Acceleration Phase Detector Gain)</td><td>0</td><td>12 Bit Offset Binary</td><td>This is the gain of the upper channel A. The value is a 12 bit offset binary number where
0x0000 is a gain of −1.0
0x0800 is a gain of 0.0
0x0FFF is a gain of +1.0</td></tr>
<tr><td>Channel A Offset
(Acceleration Phase Detector Offset)</td><td>1</td><td>12 Bit Offset Binary</td><td>This is an offset of the upper channel A. The value is a 12 bit offset binary number where
0x0000 is an offset of approx. −2.5 V
0x0800 is an offset of 0.0 V
0x0FFF is an offset of approx. +2.5 V</td></tr>
<tr><td>Channel B Gain
(MI Phase Detector Gain)</td><td>2</td><td>--
Offset Binary</td><td>This is the gain of the lower channel B.
<table>
<tr><th>Direct Feedback Mode
12 Bit Offset Binary</th><th>Reference Error Curve Mode
14 Bit Offset Binary</th></tr>
<tr><td>0x0000 is a gain of −1.0</td><td>0x0000 is a gain of −1.0</td></tr>
<tr><td>0x0800 is a gain of 0.0</td><td>0x2000 is a gain of 0.0</td></tr>
<tr><td>0x0FFF is a gain of +1.0</td><td>0x3FFF is a gain of +1.0</td></tr>
</table></td></tr>
<tr><td>Channel B Offset
(MI Phase Detector Offset)</td><td>3</td><td>12 Bit Offset Binary</td><td>This is an offset of the upper channel B. The value is a 12 bit offset binary number where
0x0000 is an offset of approx. −2.5 V
0x0800 is an offset of 0.0 V
0x0FFF is an offset of approx. +2.5 V</td></tr>
<tr><td>Curve Memory Starting Address Offset</td><td>4</td><td>8 Bit Unsigned</td><td>In the Reference Error Curve Mode for the MI phase lock, this value is the offset from the start of the reference curve memory. See the section describing this MI phase lock mode.</td></tr>
<tr><td>MI Phase Lock Gain and Ref. Curve Time Scaling</td><td>5</td><td>14 Bit Unsigned</td><td>Channel A and Channel B Gain Curve Time Scaling
0x100   =>   800 us transition interval
0x080   =>   400 us
0x040   =>   200 us
0x020   =>   100 us</td></tr>
</table>

			0x000 => Immediate Transition
MI Phase Lock Integral Gain	6	14 Bit Offset Binary	Integral gain setting used with each MI phase lock mode. The MI PD Error is accumulated from the start of MIPL and multiplied by this gain.
Mode Select	7	16 Bit	Selects different options and modes of operation for transitioning from the Acceleration phase lock and executing the MI phase lock. See the Mode Select figure below.
reserved	8		
NO_BEAM_OFFSET	9	14 Bit Offset Binary	This offset nulling value is applied to the Acceleration Phase Detector output when there is No Beam. It ensures that there is not an offset applied to the Frequency Source when doing MI phase lock test without beam, and can also zero the phase detector output just before the acceleration cycle begins.
reserved	10		
Phase Error Scaling	11	14 Bit Offset Binary	Used with the Reference Error Curve Mode for the MI phase lock. See the section describing this MI phase lock mode.

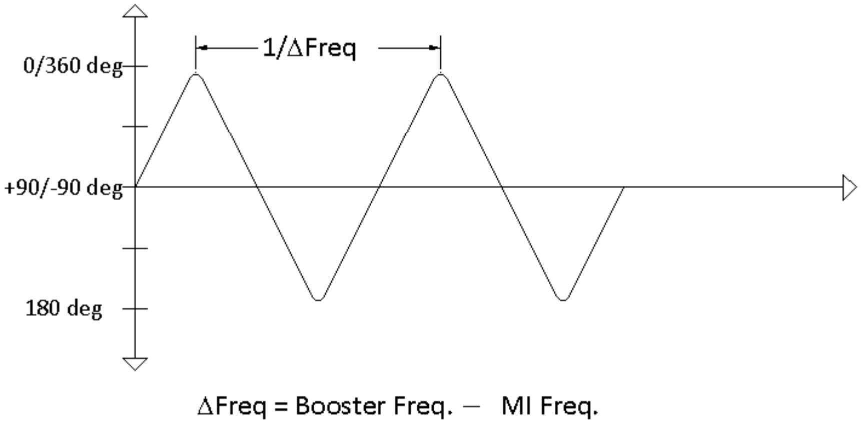
Note: Momentarily pressing the RESET button on the front of the phase detector module will cause an LED on the Programmer/Monitor Unit to blink and cause all of the programmable registers to be written into non-volatile memory. Pressing and holding the RESET button for more than a full second or two will cause the whole module to be reset and current contents of the Flash memory to be reloaded into the parameter registers.

III. MI Phase Lock, Reference Error Curve Mode

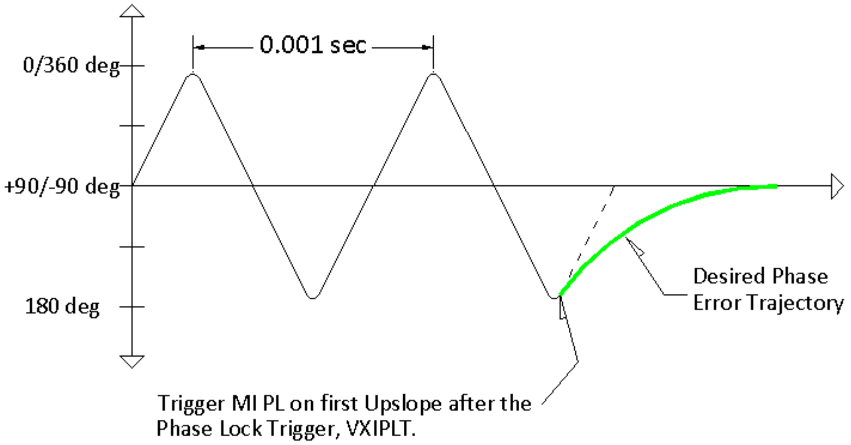
The MI Phase Lock Reference Error Curve Mode is a control method similar to the one originally used for phase locking the Booster LLRF frequency reference (and beam) to the MI frequency. The idea is to create a trajectory we wish the phase error to follow as it is being phase locked to the MI frequency. A block diagram of the method is given in Figure III.1.

The process proceeds as follows

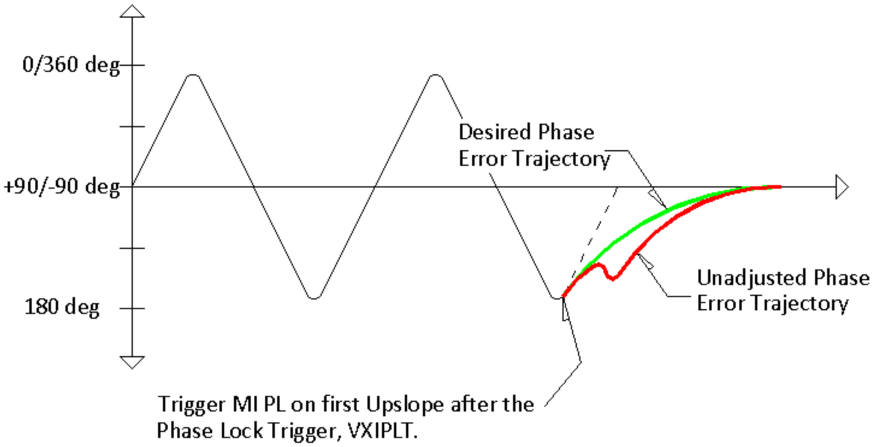
1. As the Booster LLRF frequency ramps towards the MI frequency the period of the triangle-wave output of the phase detector increases. The frequency source detects when it has reached a frequency out, 1000 Hz below the typical MI frequency of 52.813 MHz (52.812 MHz), and puts out a “begin phase lock” trigger.



2. When the Dual Phase Detector Module sees this trigger the phase lock process begins on the next upslope of the phase detector output.
3. At the start of the phase lock process the phase detector phase error value is latched in one branch of the process and this starting value is subject to scaling by the Error Reference Gain Curve. The multiplication product, which changes from the original latched phase error to zero, according to the reference curve, becomes the desired phase error trajectory.
4. The changing phase error (not latched) is subtracted from the reference trajectory to produce the error signal used in our control loop to drive the actual phase error to follow this desire reference trajectory.

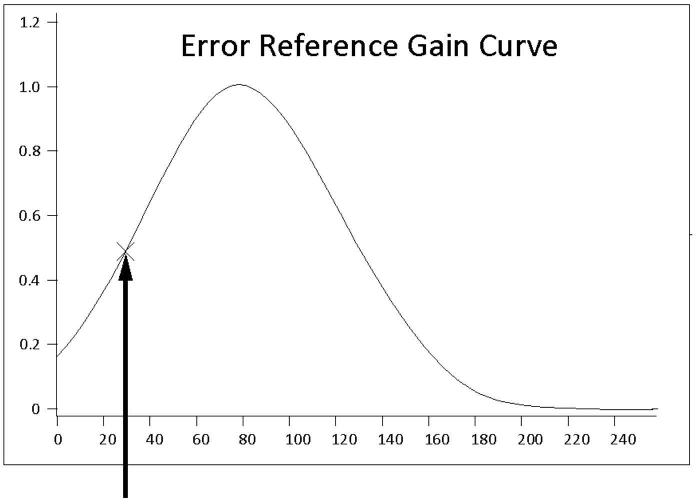

0.001 sec
0/360 deg
+90/-90 deg
180 deg
Desired Phase
Error Trajectory
Trigger MI PL on first Upslope after the
Phase Lock Trigger, VXIPLT.

5. Adjustment is needed in this process to compensate for the fact that since the phase error we are trying to force to follow our desired trajectory, begins with its own trajectory with a non-zero time derivative. Latencies and time constants in our control loop will cause the phase error to initially “backup” to get on-track with our desired trajectory that begins at the phase error latched at the beginning of the process.



6. In order to present a trajectory that the phase error can smoothly follow we apply a gain curve that initially increases the latched phase error before driving the trajectory to zero. The first adjustment to smoothing the resulting phase error trajectory is to change where on the rising side of our reference gain curve that we begin.

7. The second adjustment matches the scale of the incoming phase error to the scale of the point where we start in our reference gain curve. That is our reference gain curve is normalized to be between 1 and 0. If we do not start at the peak of the gain curve we initially apply a gain less than 1 and we want to apply the same gain to the incoming phase error so when the phase error and trajectory are compared the difference is initially zero. The overall reduction in the feedback gain is compensated for by the control loop gain settings.



Curve Memory Starting Address Offset

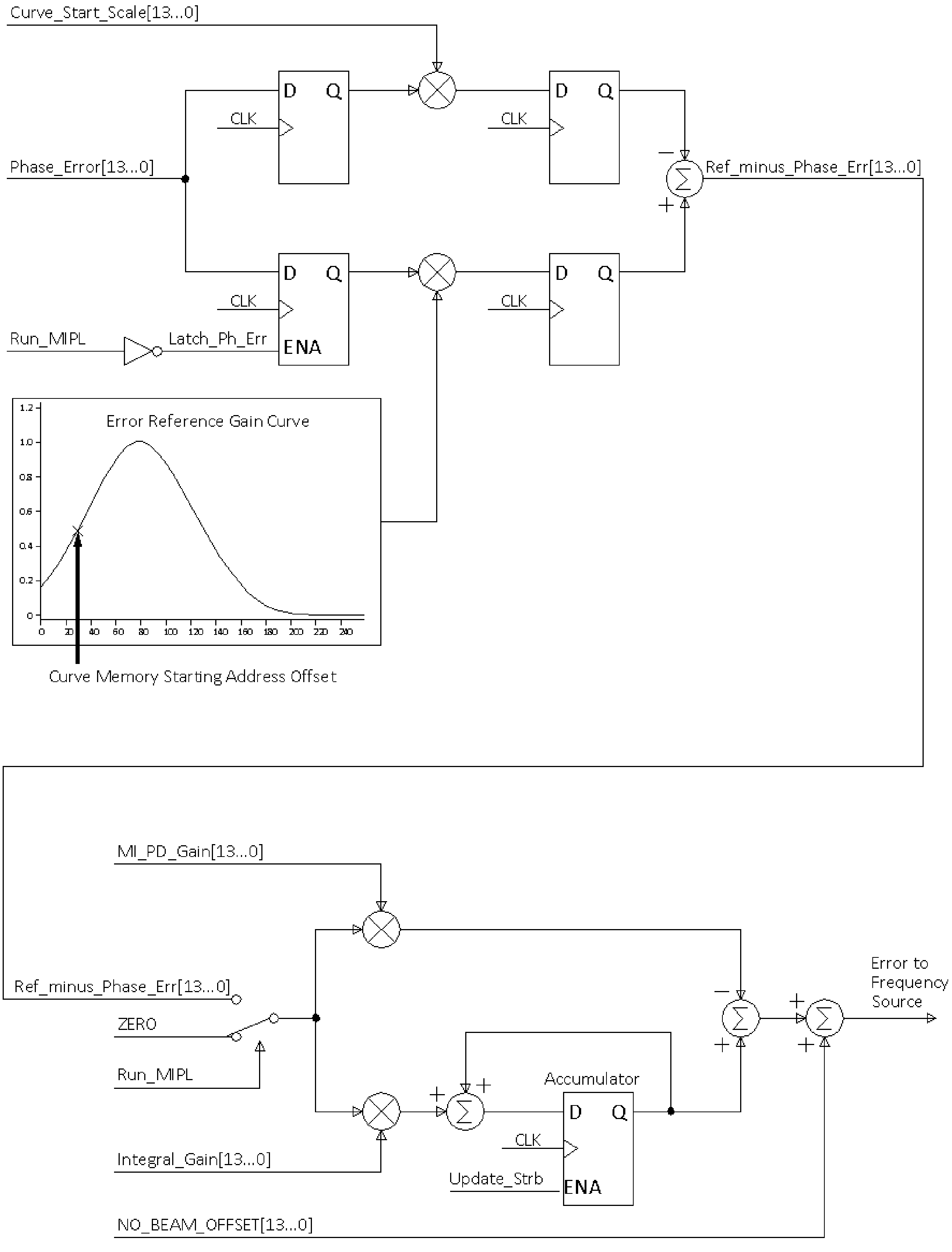


Figure III.1 Block diagram of the Reference Error Curve Mode processing.

This method of generating a reference trajectory and driving the LLRF frequency to follow this trajectory is sensitive, but not overly sensitive, to the frequency difference between the Booster RF and the MI RF at the start of the phase lock process. Nominally, we expect this difference to be 1000 Hz. Currently, we expect to still get good results between a frequency difference between 2500 and 500 Hz.