XFR Modification to Resetting

Beam Sync (AA) and Offset Beam Sync (OAA)

And Simulation and Test Results

Version 2

Craig Drennan

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# Version 2

This note describes Version 2 of the Booster to MI/RECYCLER reset delay. In addition to using the Bucket Offset setting to fix the relationship between the reset signal and the OAA markers, the logic also ensures the “first” OAA after a reset appears with a fixed offset from the reset for all resets from 0 to 587. The previous document dated April 29, 2015 described a discrepancy between beam sync offset setting below 7 and those 7 or greater.

# Introduction

If you are already familiar with what the Beam Sync and Offset Beam Sync are you should probably just skip the rest of the introduction unless you are interested in helping me find and correct the inaccuracies in the introduction. Rather move onto Section 2.

Two beam sync, timing pulses are generated by the XFR Module. The Beam Sync (AA marker) represents Bucket Zero with respect to the injected beam into the Main Injector/Recycler. The Offset Beam Sync (OAA marker) pulse occurs some number of RF counts or some bucket offset after the Beam Sync. The OAA marker is used by the Booster to compute when a Booster beam batch is to be extracted from the Booster so that it arrives at the MI/Recycler at the proper time to be injected at the desired bucket offset.

Several Booster cycles of beam, or batches, are injected into the MI/Recycler. Each batch of beam is inserted, injected into the MI/Recycler just behind the previous one. Once the desired number of batches have been delivered from the Booster into the MI/Recycler, the Booster either pauses or sends beam elsewhere while the MI/Recycler accelerates the beam it received and then delivers the beam to an experiment.

When the Booster is accelerating the first batch of beam, into an empty MI/Recycler, the Booster timing will predict when it is going to be extracting this first batch and sending a Beam Sync Reset signal (MI Reset). The prediction is made and the reset signal sent near the end of the acceleration cycle. This reset, in conjunction with the Bucket Offset establish the location of Bucket Zero, the AA marker and the OAA marker. The MI Reset signal is timed with respect to the predicted Booster extraction such that the OAA marker is retimed to occur when the first Booster batch of beam is injected into the MI/Recycler. The OAA marker established at the end of the first batch is used to time the extraction of the remaining Booster batches

# Generation of Beam Sync and Offset Beam Sync Signals

The Beam Sync (AA) and the Offset Beam Sync (OAA) are generated by the XFR VXI electronics module in the Altera FPGA U18. Figure 2.1 is a *loose* illustration of the timing involved. The MI Reset signal is received by the XFR module and is synchronized to the MI/Recycler RF Clock. There is a fixed number of clocks between the reset and the AA marker. The Bucket Offset is an ACNET variable that defines the number of clocks between the AA marker and the OAA marker.

In order for the Booster timing logic to produce the MI Reset such that the resulting OAA marker is positioned with a fixed relationship to the injection of the first batch of beam into the MI/Recycler the Booster timing logic must know the Bucket Offset. This is the difficulty that we wish to remedy with the proposed modification.

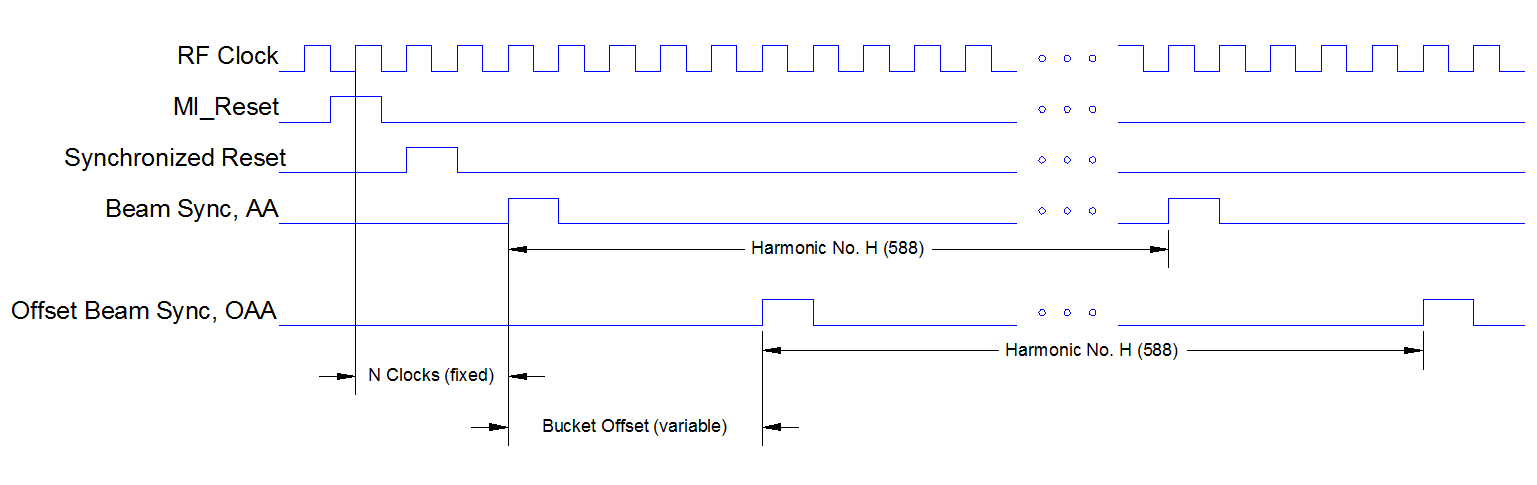


Figure 2.1 Timing of Beam Sync signals.

Currently if the MI/Recycler operators wish to change the Bucket Offset the Booster timing logic must be modified. The current Booster Cogging Controller logic has been patched to be able to do this, but a new Cogging Controller has been developed and it is a good time to consider a better way. If the Bucket Offset could be changed without having to modify logic in the Booster, this would give MI/Recycler operators more freedom in choosing it.

# Proposed Modifications

## Simplified Description of Added Delay Logic.

One possible change would be to send the Bucket Offset, set at the ACNET console, to both the XFR VXI Module and the Booster timing logic. Guaranteeing that the Offset value is updated in two places on the same cycle is difficult. Not updating the Offset in both places would cause significant beam loss.

The solution we are proposing is to make a simple modification to the logic in the XFR VXI module to delay the MI Reset a number of clocks based on the Bucket Offset setting. The MI Reset will be delayed such that the number of RF Clocks between the reset and the next OAA marker will be a fixed value independent of the Bucket Offset setting. Figure 3.1.1 is a simple timing diagram showing the delay between the MI Reset and the Delayed Reset.

The logic to produce the Offset Reset is shown in Figure 3.1.2. A simple simulation of this logic is shown in Figure 3.1.3.

Figure 3.1.4 gives an indication of where in the existing logic the Reset Delay block would be inserted.

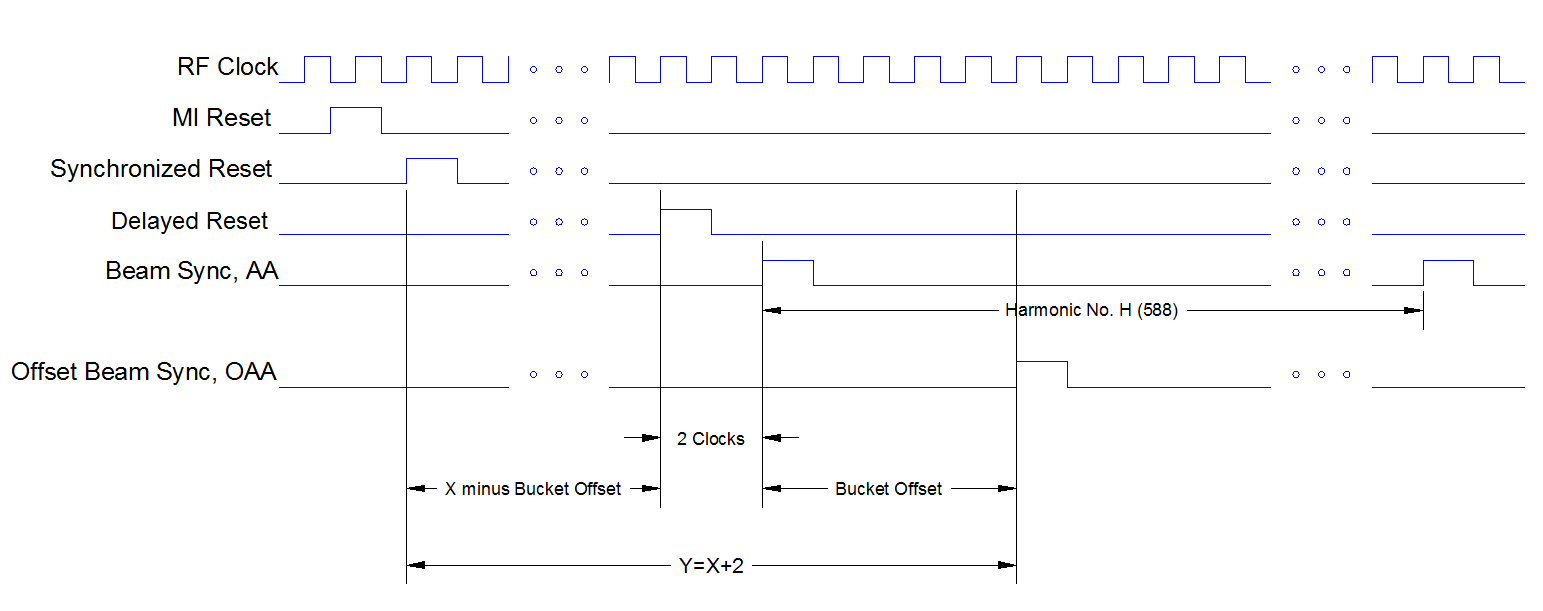


Figure 3.1.1 Simplified Timing for the new Delayed Reset

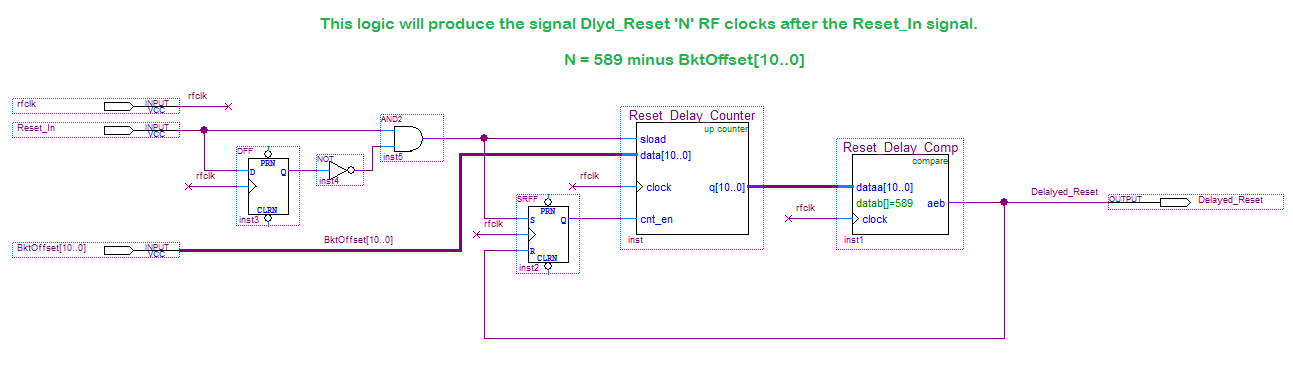


Figure 3.1.2 Simplified Reset Delay Logic

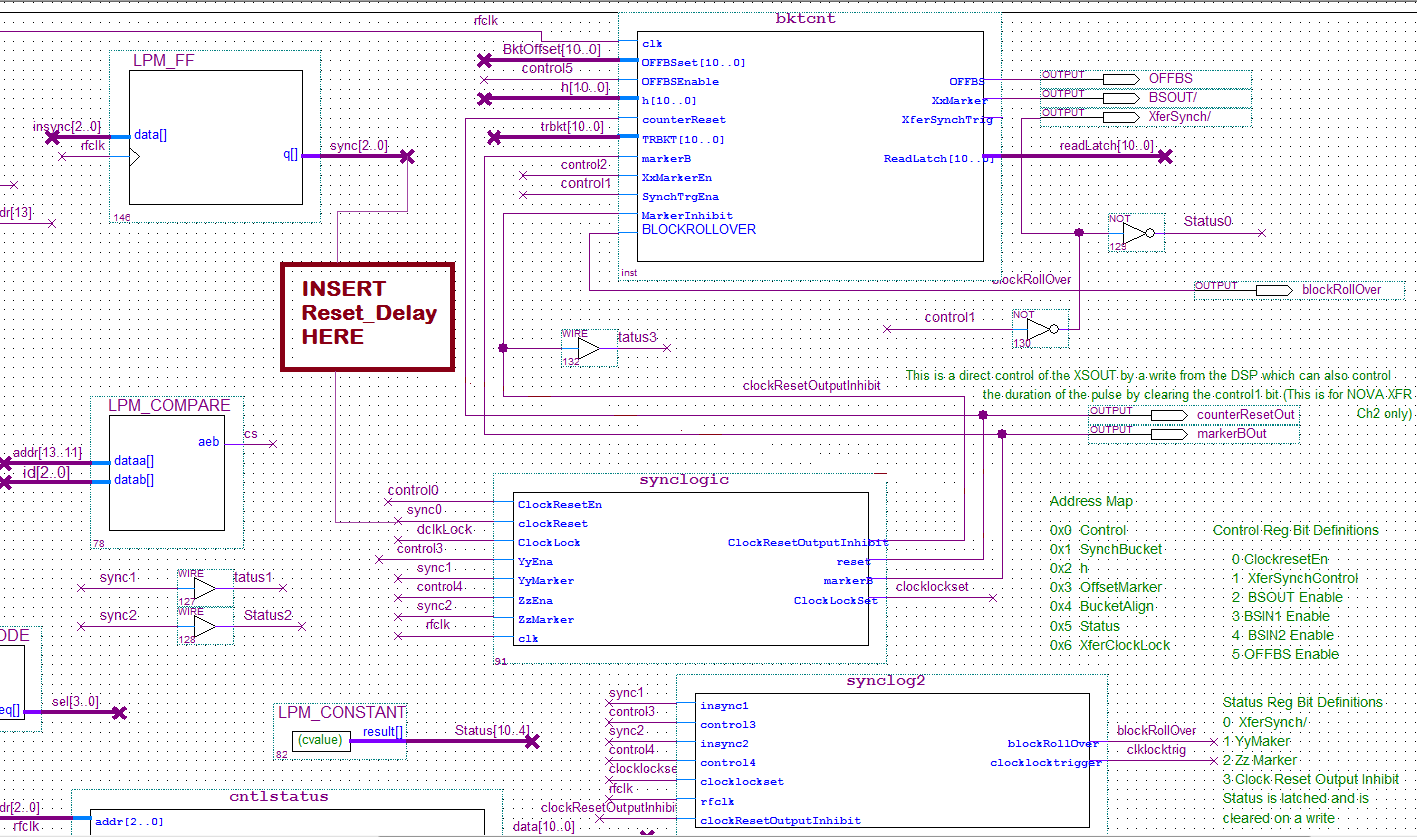


Figure 3.1.4 Indication of where in the existing logic the Reset Delay block would be inserted

## Handling Offsets Below 7 and Those 7 or Greater

The designers of the existing logic use an rf bucket counter that starts at 6 when the reset is applied. Starting the count at 6 compensated for delays introduced by other synchronous logic elements in the signal path. The counter counts to 587 and rolls back to zero. After rolling back to zero it counts back up to 587 and repeats. Each time the count is rolled back to zero the Beam Sync, AA marker is generated. Each time the count reaches the Beam Sync Offset setting the Offset Beam Sync, OAA marker is produced. You can see that if the Beam Sync Offset is greater than 6 the OAA is produced before reaching the 587 count and before rolling back to zero and the appearance of the first AA marker. If the offset is 6 or less the counter counts up to 587, rolls back to zero, the AA marker is generated, and then the first OAA marker is produced.

We have chosen the method shown in Figure 3.2.1 to accommodate these two cases.

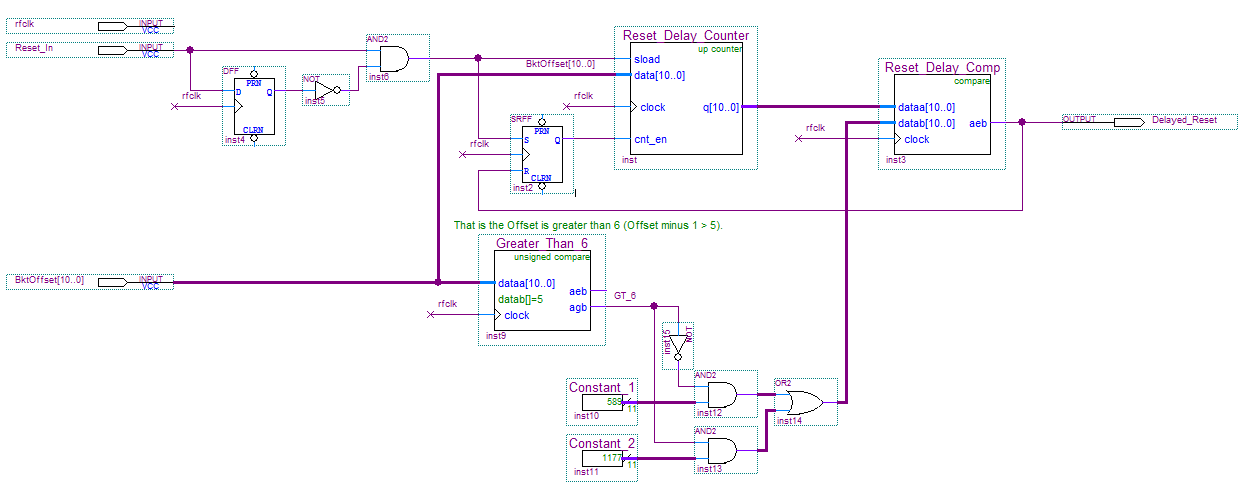


Figure 3.2.1 Version 2 of the Reset Delay Logic.

The total delay between the Booster MI Reset and the first OAA marker is the sum of the rf bucket counter counting between 6 and the marker offset setting,

And the new reset delay logic,

The sum in both cases is then,

Further, we can consider all of the synchronization and other clocked logic from the reset input to the OAA marker output. This is, for the current modified logic, 7 to 8 rf clocks. So the final delay is

# Logic Testing

## Altera FPGA Configuration

There is a single EPROM configuration device on the XFR Module that programs three FPGA’s. U18 is the timing logic for Channel 1, U19 is the timing logic for Channel 2 and U20 decodes MDAT. When programming a new configuration EPROM, the code for all three FPGA’s must be combined into a single \*.pof programming file with which to burn the EPROM. The Altera Stat Sheet that describes how an EPROM was programmed is given in Listing 4.1

Module Name: XFR

(Recycler Nova U19 version Plus Booster Reset Delay U18 version)

Files to be found @

[\\beamssrv1\rf.bd\projects\LLRF\Components\Hardware\Altera](file:///\\beamssrv1\rf.bd\projects\LLRF\Components\Hardware\Altera) files\XFR\xfru21\_Booster\_Nova\

Maxplus or Quartus version compiled last: Quartus 9.0

Project name: XFRU21\_Booster\_Nova

Compilation Date: 05/6/2015

Device type: EPF10K20TC144-3

Programming files (POF and/or SOF): cogging.sof (NEW file for U18)

Cogging\_nova\_Ch2.sof (file for U19)

U20.sof (file for U20)

xfru21\_B\_N\_v2.pof (pof resulting from the combination)

POF Checksum: 00BC9AF0

Listing 4.1 Altera Stat Sheet data for programming the EPROM.

## Test Stand Setup

The AD/RF Group maintains VXI test crates, processors and test code for testing and maintaining Main Injector VXI RF modules such as the XFR. The crate/processor environment used for testing the XFR was running in sync with the MI TClk’s and MDAT States. The Booster typically sends the MI Reset signal near the end of the Booster cycle producing the first batch of beam to the MI. The first Booster batch cycle is typically the first $19 event following the $12 event. Therefore, a function generator was setup to output a reset pulse 96 ms after the $12 event trigger. This is expected to produce the reset pulse 30 ms into the first batch Booster cycle. Measurements were made on the time offset of the first XFR OFFBS (OAA marker) with respect to the rising-edge of the reset pulse. Measurements were then made of four BSOUT (AA marker) and the remaining three OFFBS (OAA marker).

Time relationships were later adjusted to compensate for delays in the connecting cables.

Delay scope to RESETIN = 12 ns

Delay BSOUT to scope = 20.2 ns

Delay OFFBS to scope = 8 ns

Figure 4.2.1 illustrates the test setup. Figure 4.2.2 shows the ACNET page used to setup the module and set different BS Offsets.

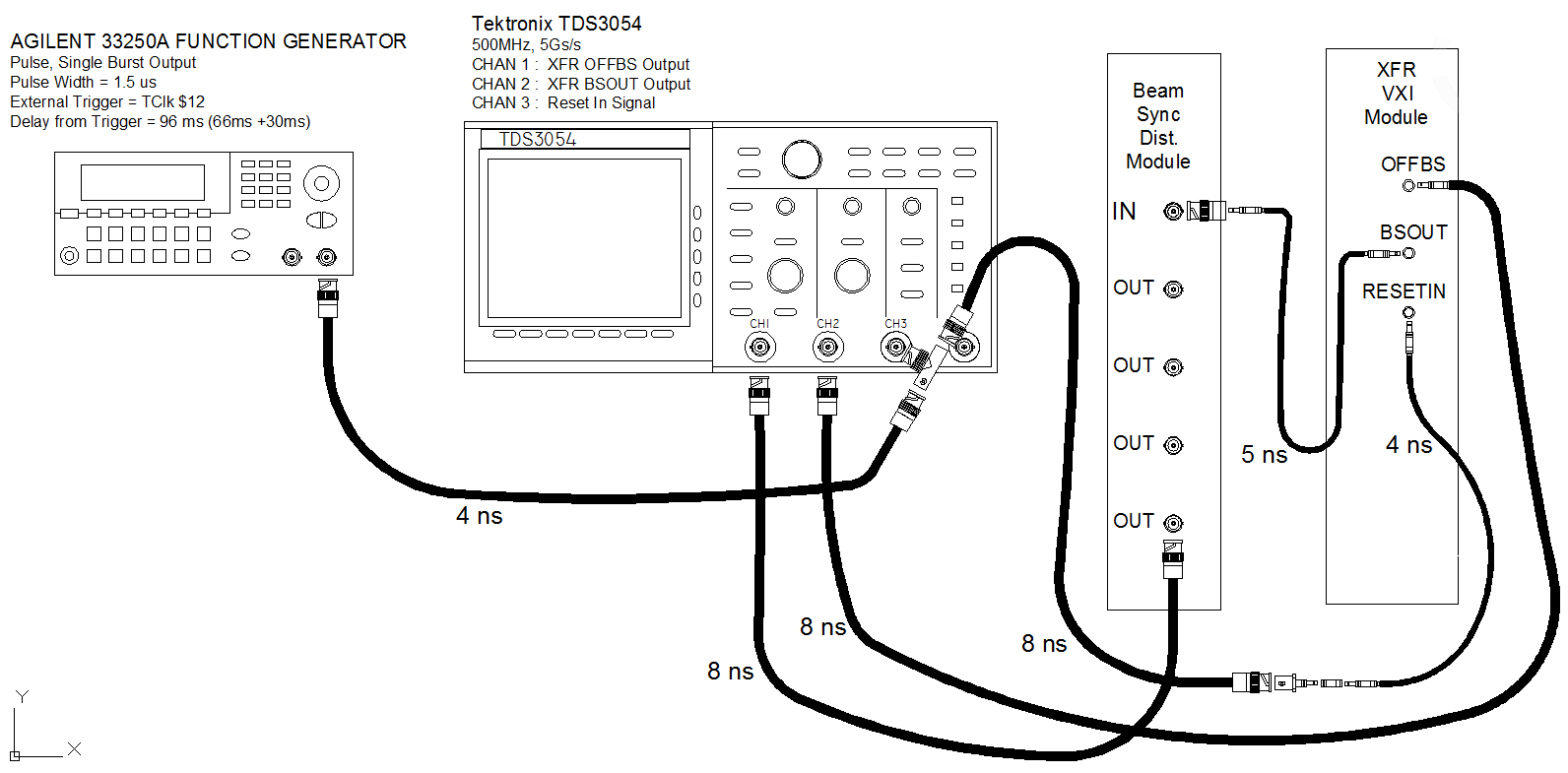


Figure 4.2.1 Test Setup

On ACNET, the R6 page was used to setup the XFR and set various BS Offsets (XferSyncRRNVtoBooster).



Figure 4.2.2 ACNET Settings.

## Test Results

The resulting marker times are listed in the tables below. In the standard XFR (un-modified) the AA markers were stationary w.r.t. the reset, at times; 11.130 us, 22.266 us, 33.394 us, etc.. The OAA markers were delayed w.r.t. the AA markers by the set offset.

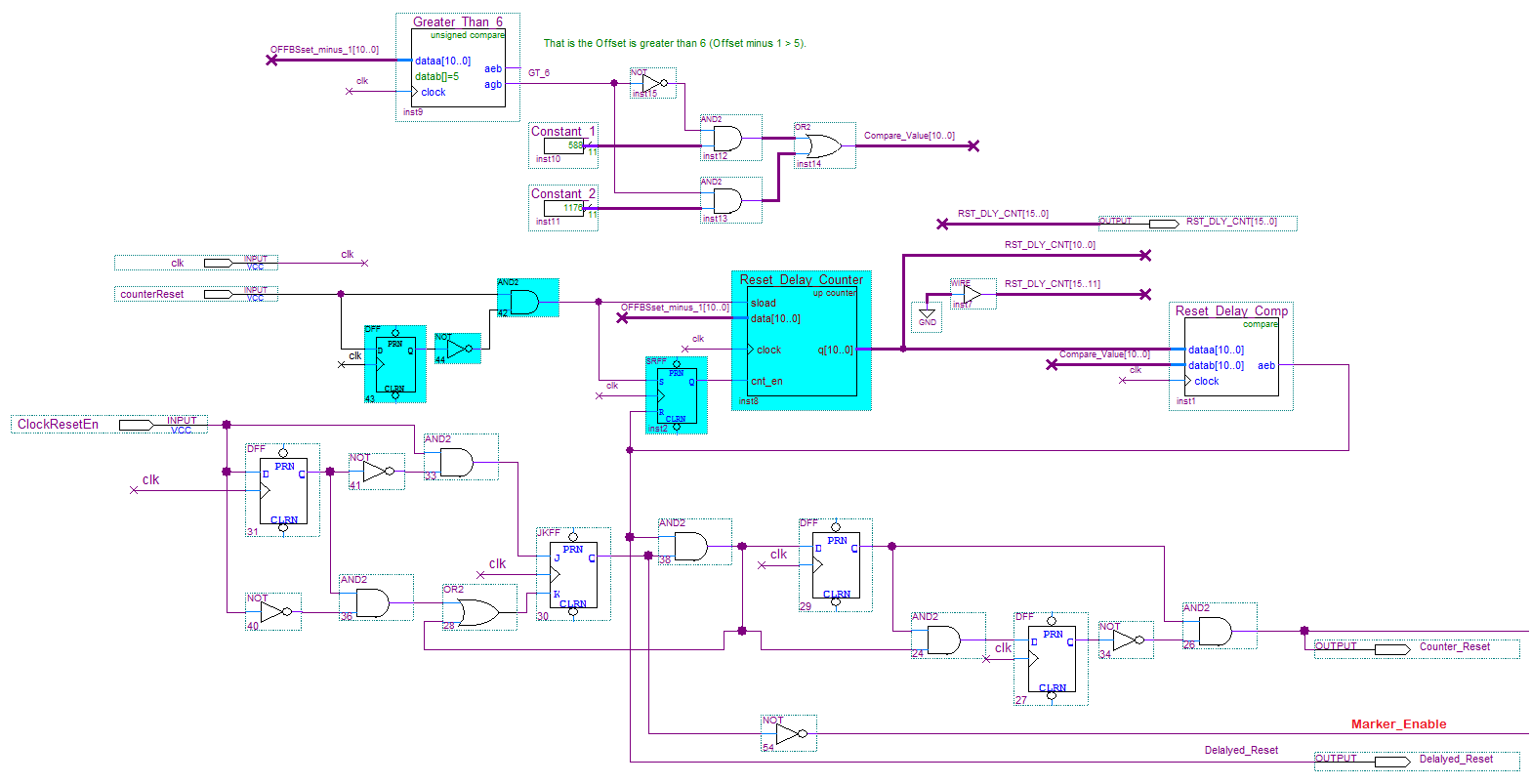




# Simulation of New Logic

Note that the harmonic number ‘h’, 588 for the MI and RR, written to the FPGA is reduced by 2 counts. The Bucket Offset written to the FPGA is reduced by 1. If the Bucket offset was originally 0 (zero) then this value is set to 587. These two values are input to 11 bit comparators. The adjustments compensate for the surrounding logic that synchronize results and reset the counter. The adjustments are made in the DSP that writes the FPGA.

Figure 5.1 is the logic used in the simulation. A careful analysis of all of the logic of FPGA U18 was made and logic paths unaffected by the Booster MI Reset signal were removed. More could have been removed, less could have been removed, but it is believed that what was retained made for a valid simulation.



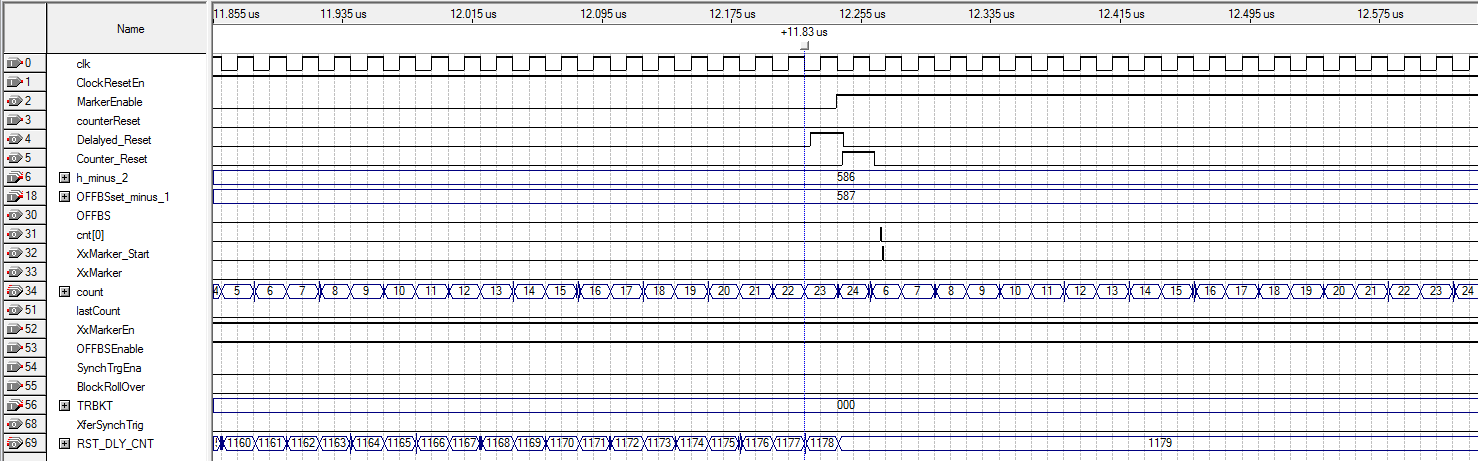
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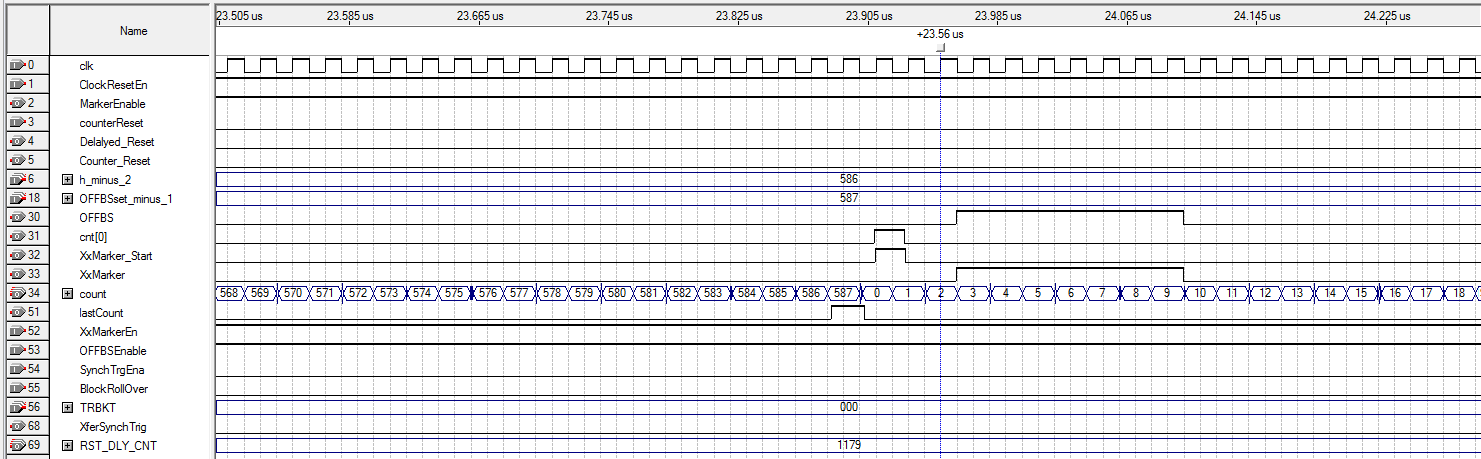


Figure 5.1 Logic used in simulation.

**NOTE THAT THE rf Clock in the simulation is 20ns for simplicity.**







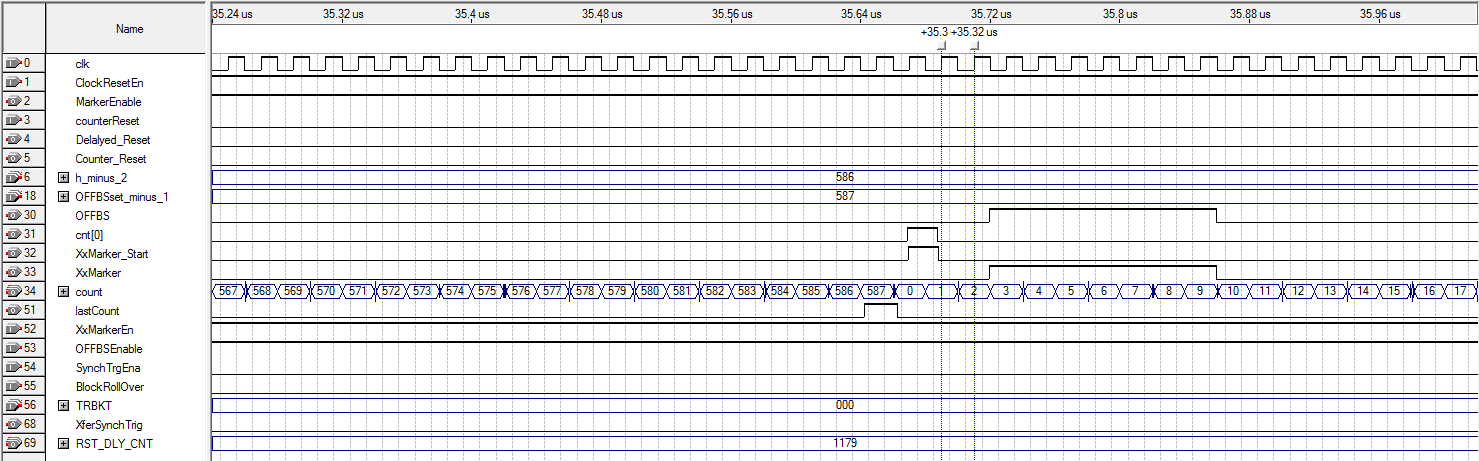
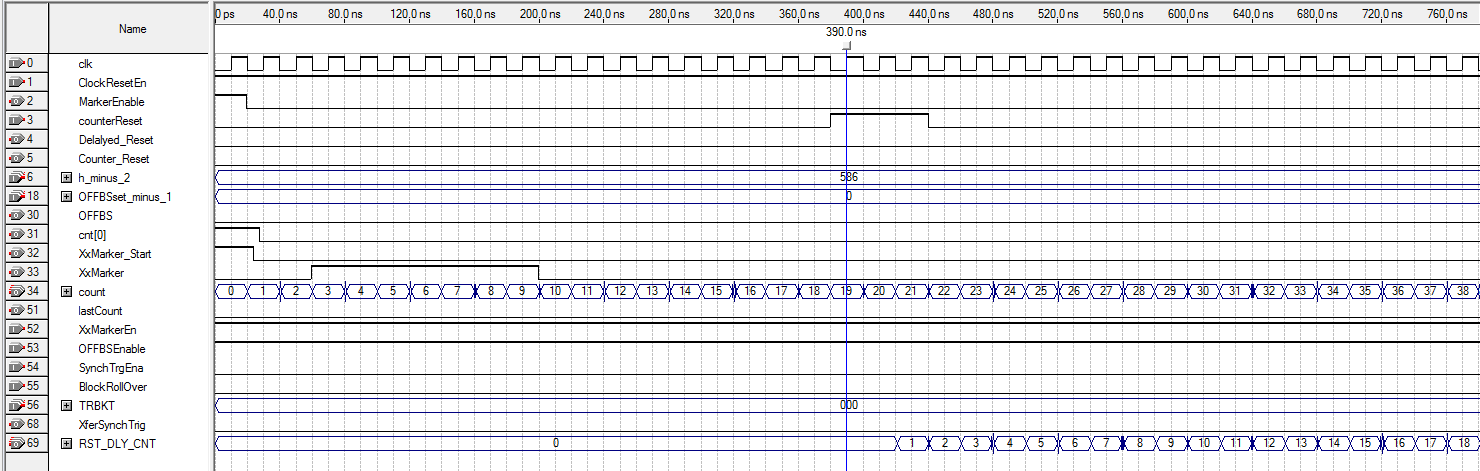
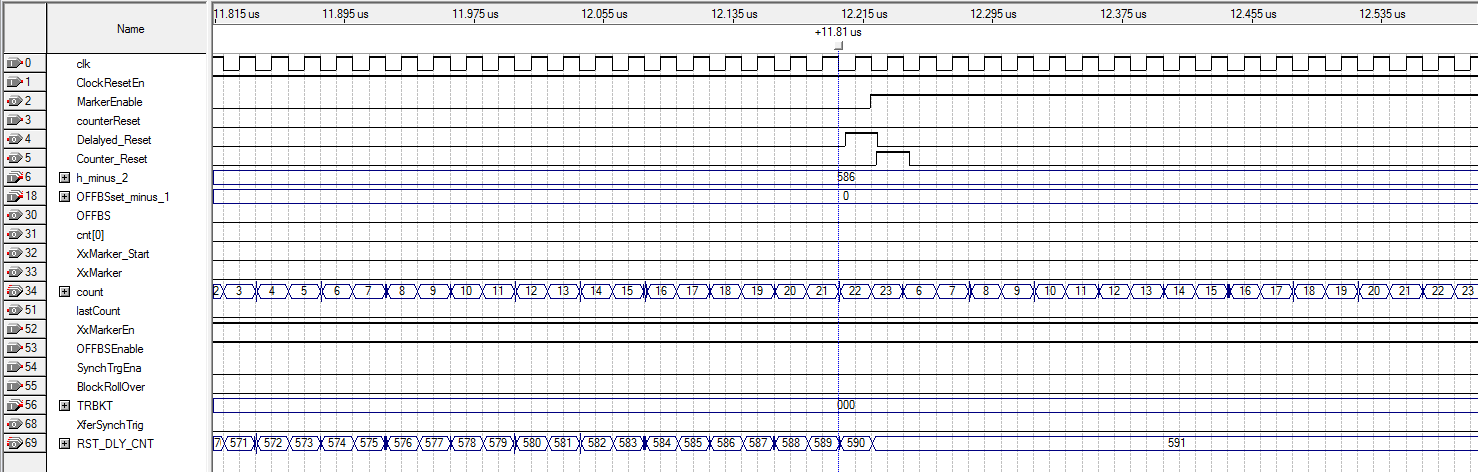
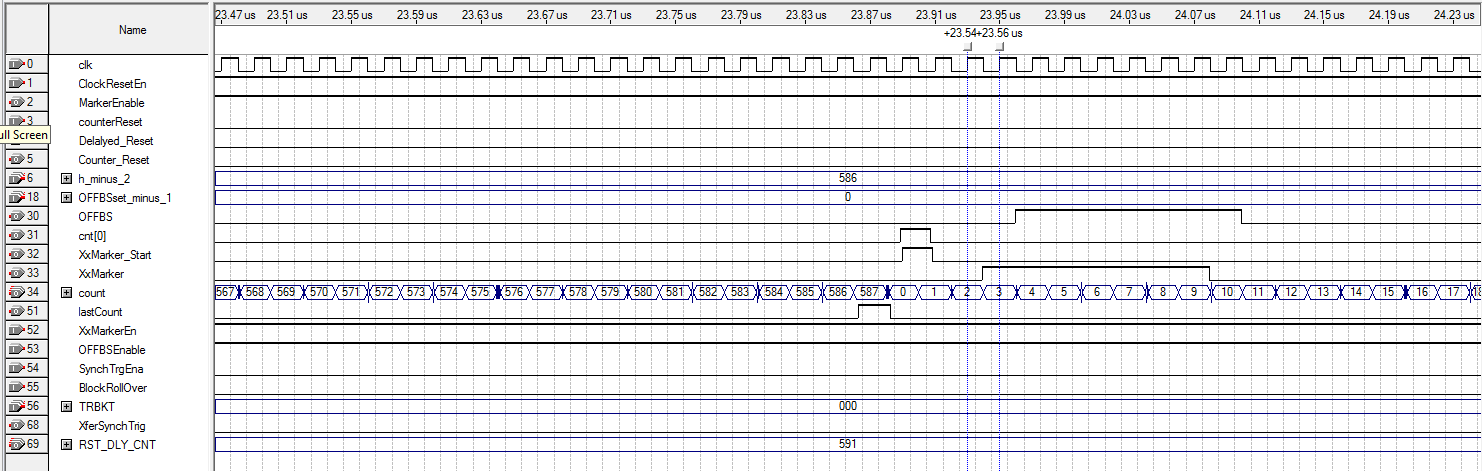


Figure 5.1 Logic Simulation for Bucket Offset of 0.







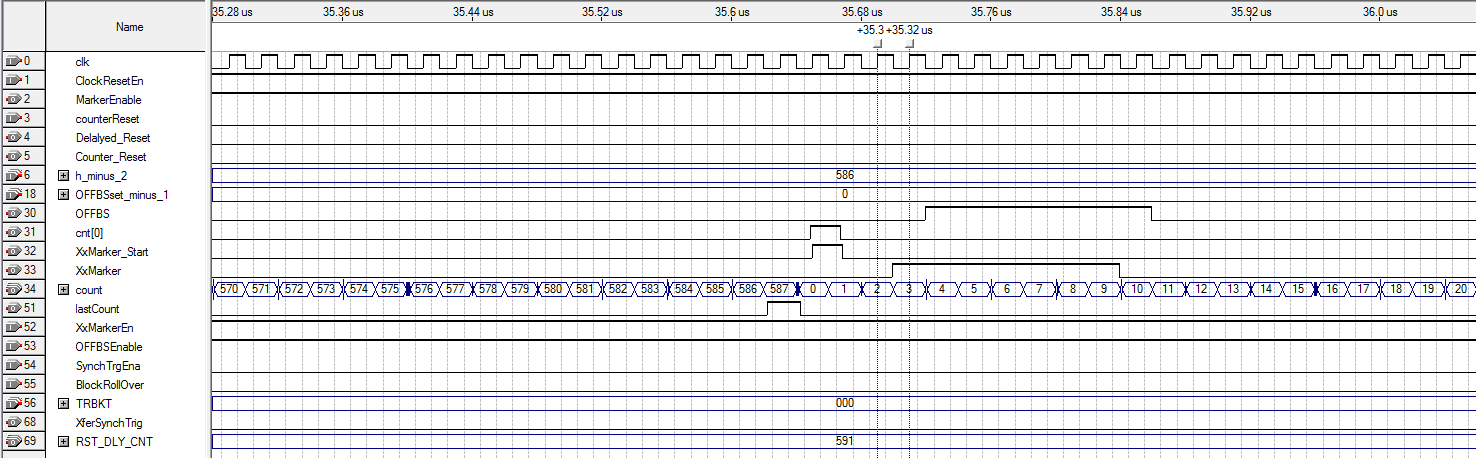
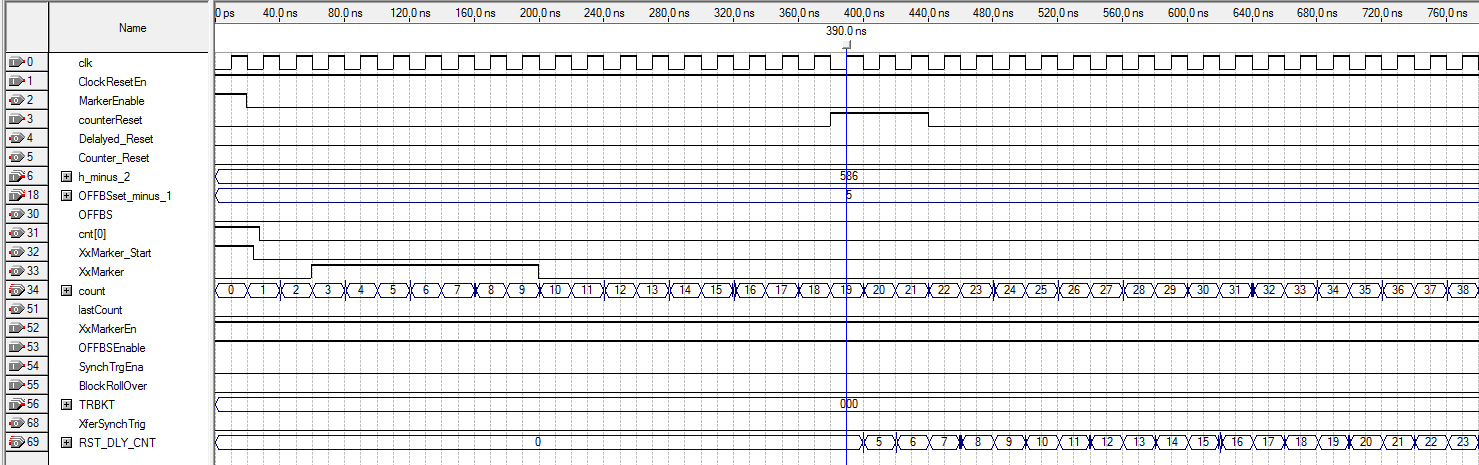
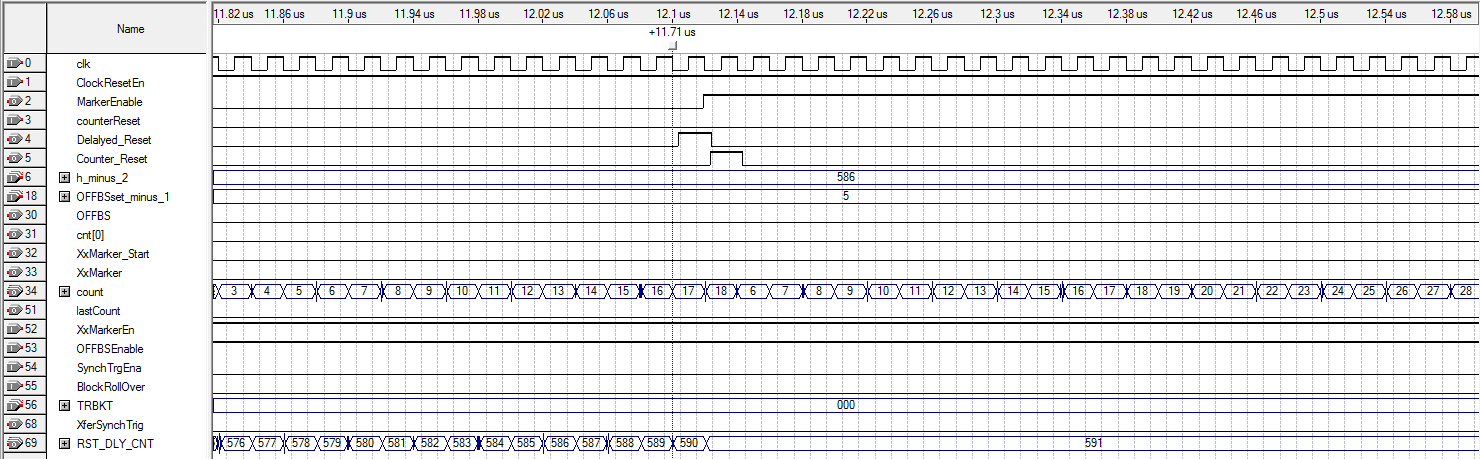
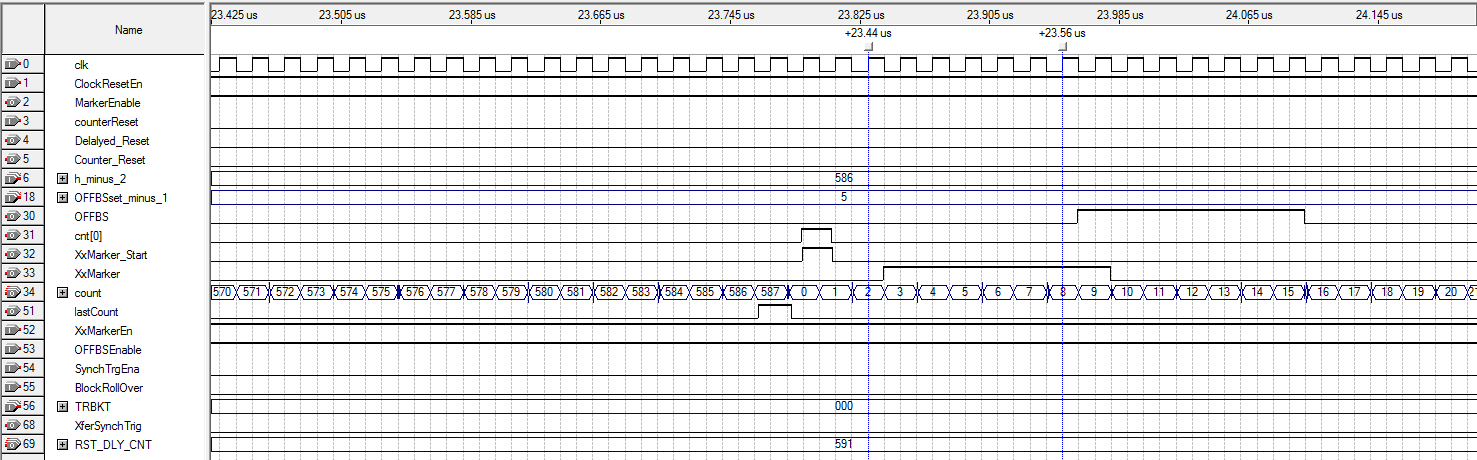


Figure 5.2 Logic Simulation for Bucket Offset of 1.







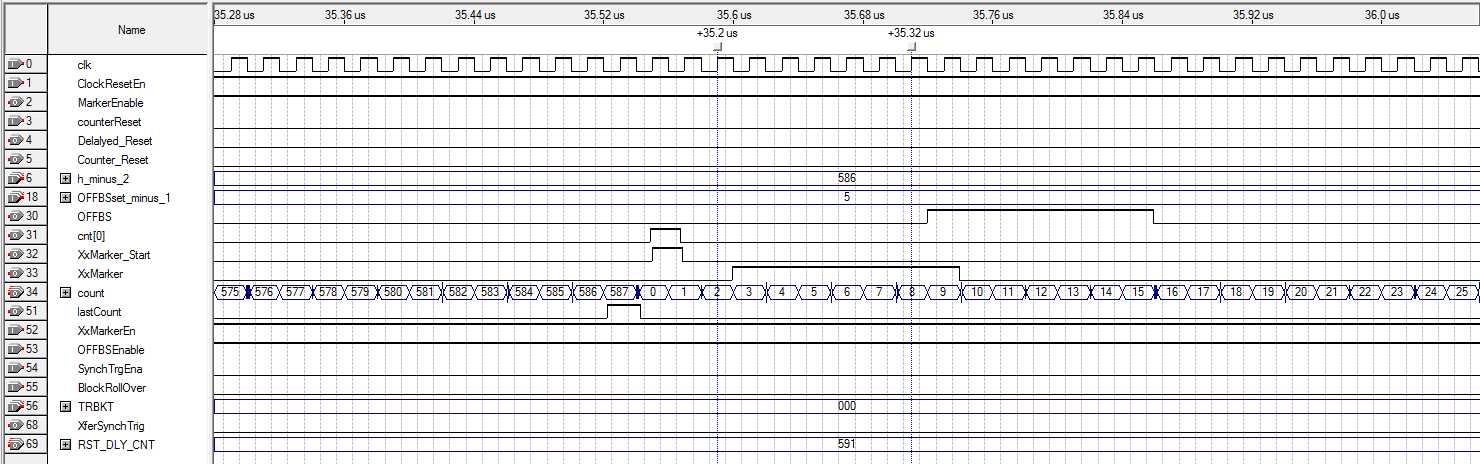
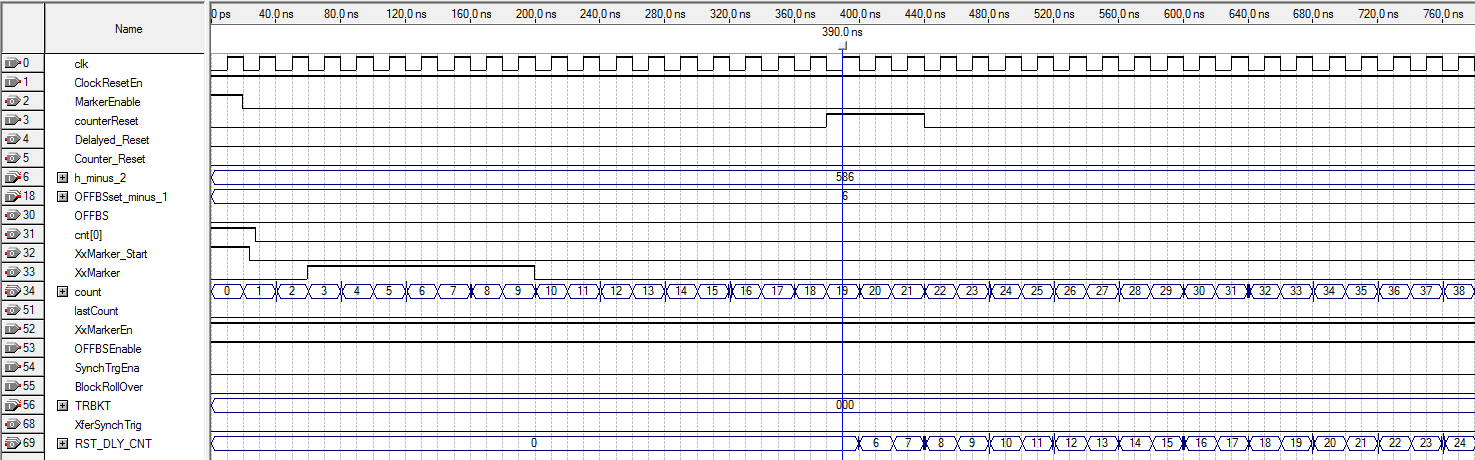
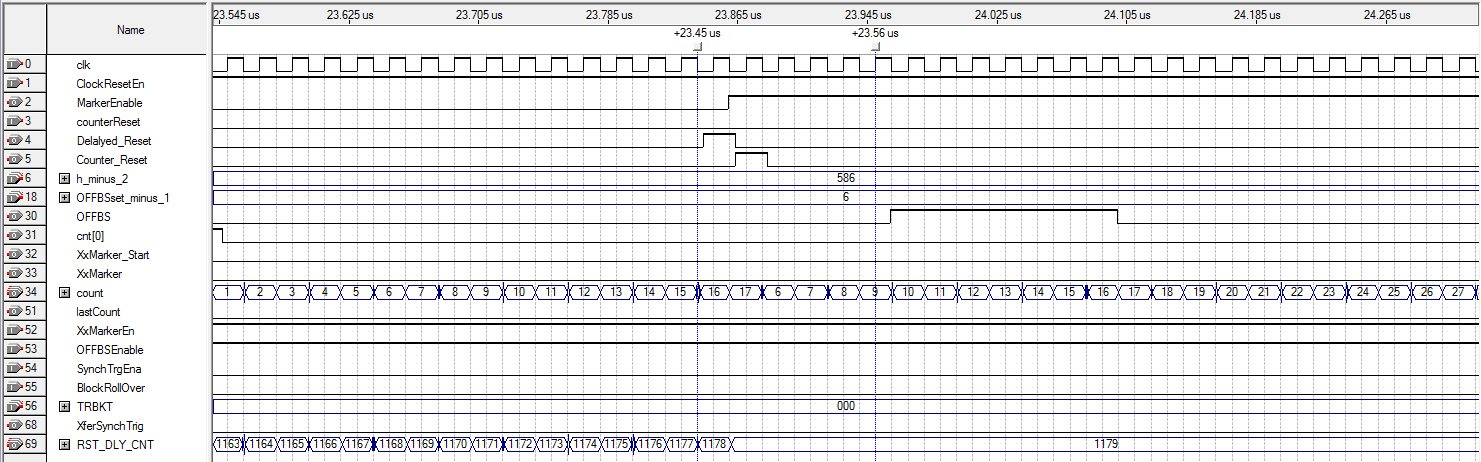


Figure 5.3 Logic Simulation for Bucket Offset of 6.





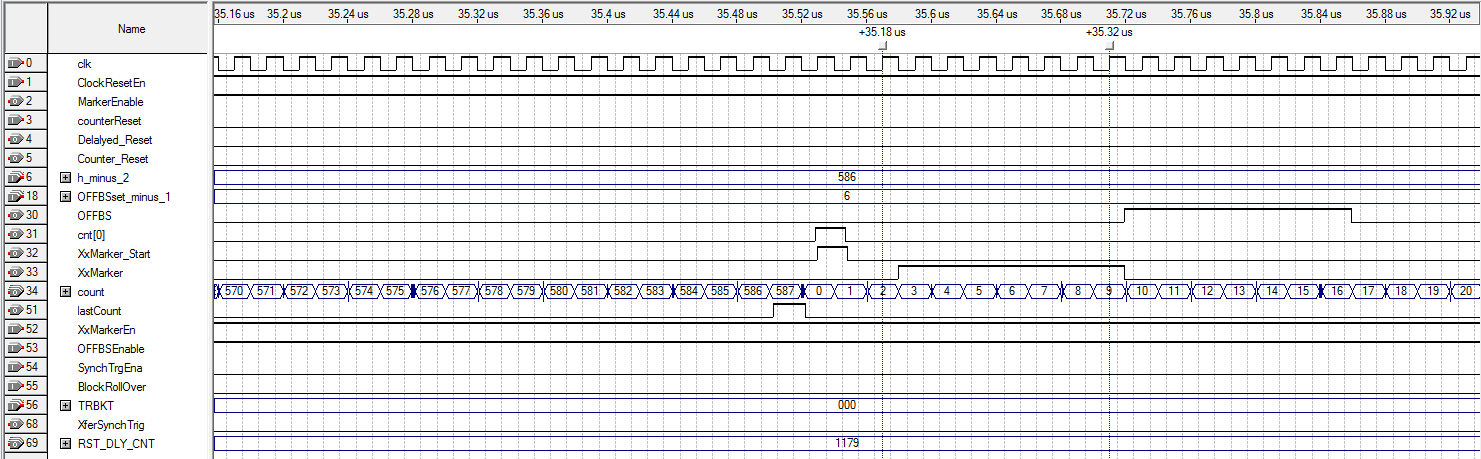
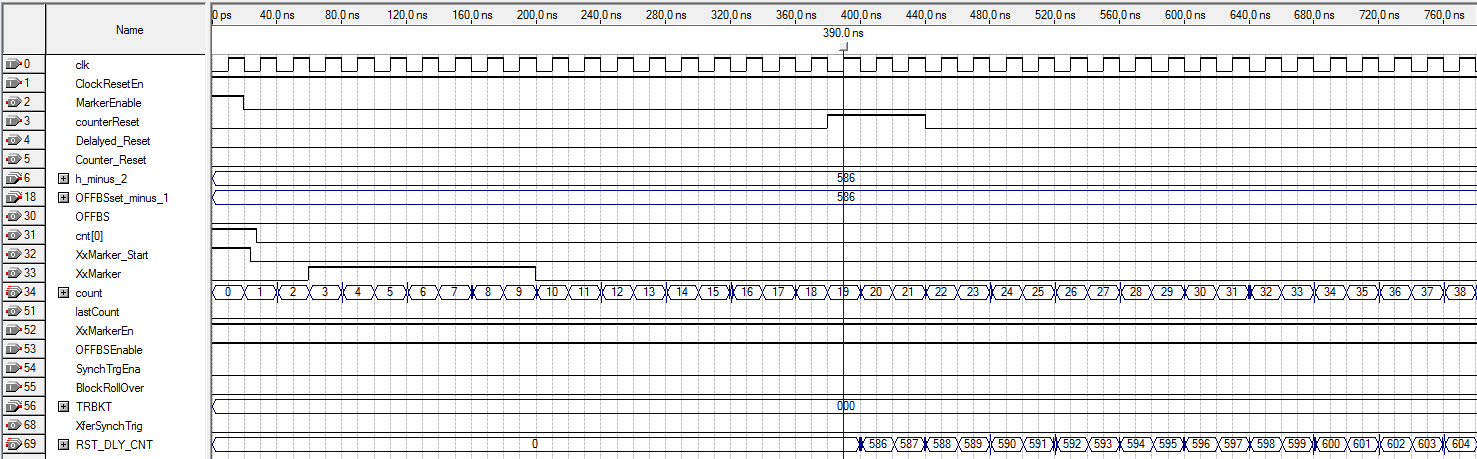
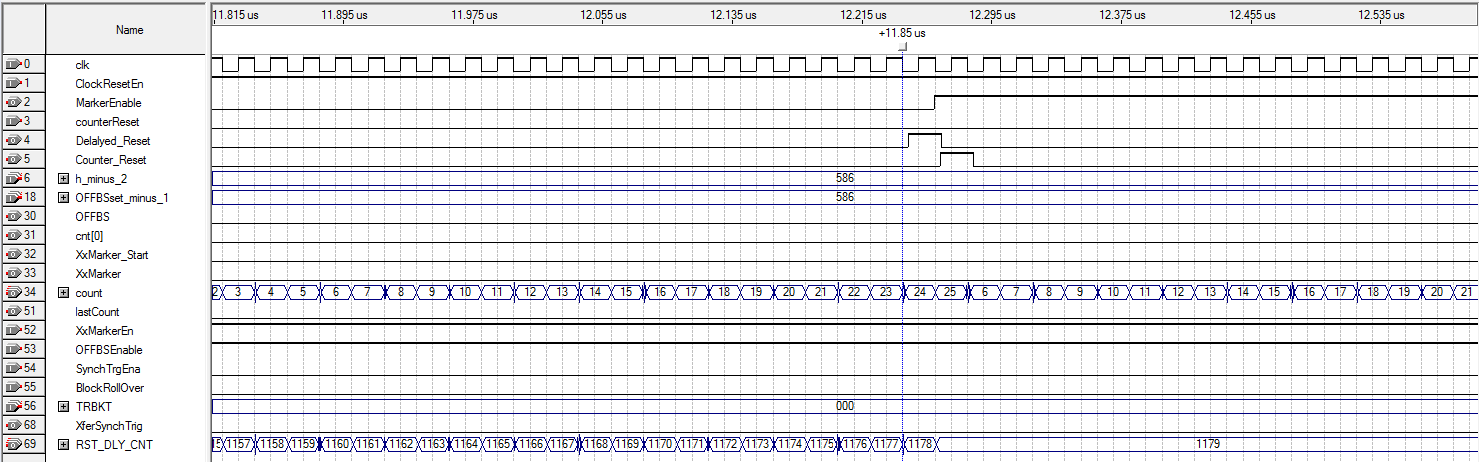
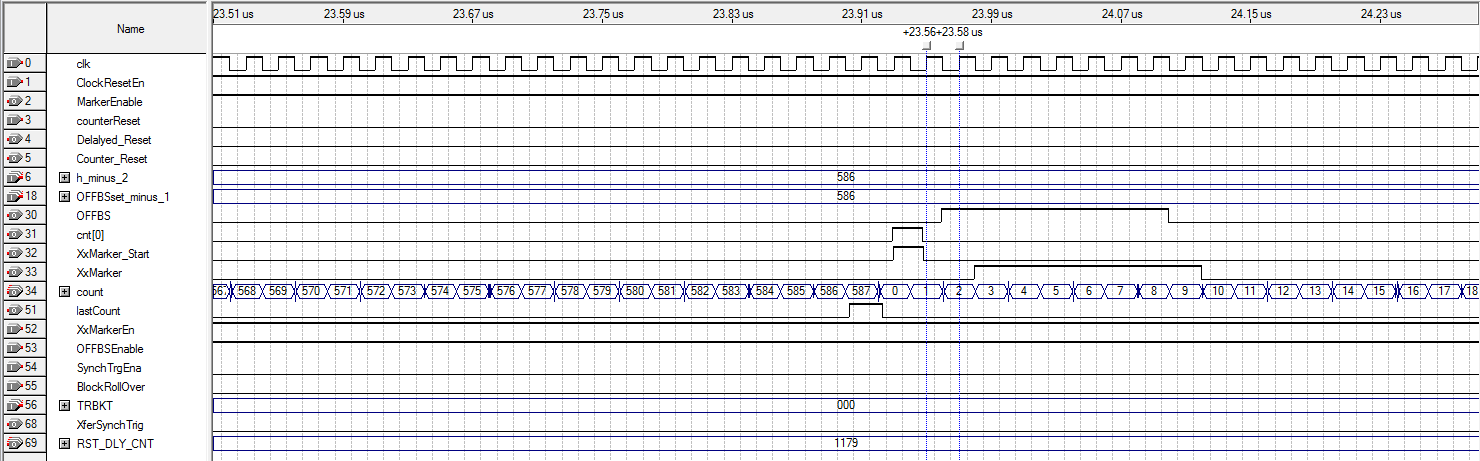


Figure 5.4 Logic Simulation for Bucket Offset of 7.







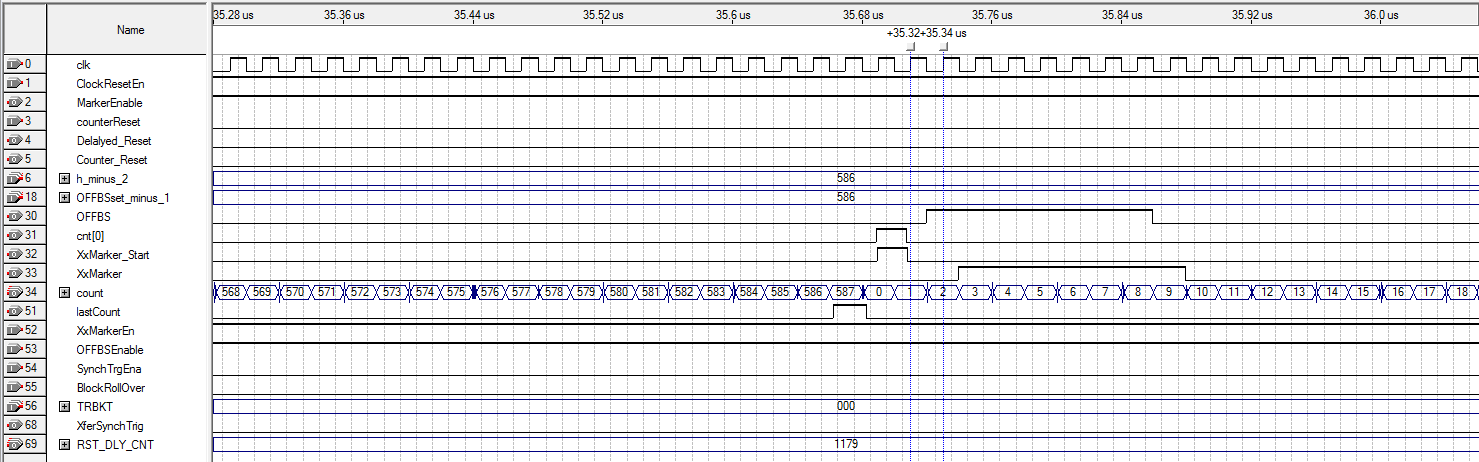


Figure 5.5 Logic Simulation for Bucket Offset of 587.