

Booster Acceleration Phase Lock Controller

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I. Introduction

One of the Booster Accelerator's main feedback control loops is the Acceleration phase lock loop that works to pull the Booster LLRF frequency reference RF and the Booster beam bunches in phase with one another as the LLRF frequency reference sweeps from approximately 37.8 MHz to 52.8 MHz. A phase detector measures the phase error between the RF and the beam. This results in a phase error voltage that is fed to the LLRF frequency reference module where it adjusts the LLRF frequency.

Four milliseconds before the end of a Booster acceleration cycle the LLRF controls switch from phase locking the LLRF reference to the beam, to phase locking the RF to the Main Injector RF. This is done by holding the phase error voltage from the Acceleration Phase Lock Controller and then summing in a phase error voltage from the Main Injector Phase Lock Controller (MIPL).

Sensitivity of the LLRF frequency to the feed back voltage is approximately 1000 Hz per 20 mVolts. The Booster beam bunches develop some amount of phase oscillation. This results in a phase error feedback signal with 20 mV to 60 mV peak to peak oscillation at about 640 kHz (1.56 us period). When holding the Acceleration phase error, the hold point can vary by the amount of the peak to peak levels. Holding the feed back value at an offset from the mean value of the oscillating phase error results in a step change in the RF frequency that is driving the beam. This sudden change in frequency results in synchrotron oscillations of the beam. If the magnitude of the synchrotron oscillations are so strong that they cannot be damped to a low level before extraction, there can be a significant phase error in the beam delivered to the Main Injector.

When these oscillations occur while switching to the Main Injector Phase Lock mode there can also be large swings seen in the Booster beam radial position. This can result in beam loss in addition to phase errors at extraction. It was found that the magnitude and direction of these swings was in direct proportion to the distance and direction from the Acceleration phase error mean, where the phase error is held.

In order to reduce the beam oscillations and the radial position swings, a scheme was implemented to bandwidth limit the phase error just before holding it at MIPL time.

II. Module Description

II.1 Module Block Diagram

The Acceleration Phase Lock Controller has an analog signal path controlled by a programmable FPGA device with a variety of IO. The block diagram of the module is given in Figure II.1.1 and descriptions of the various sections follows.

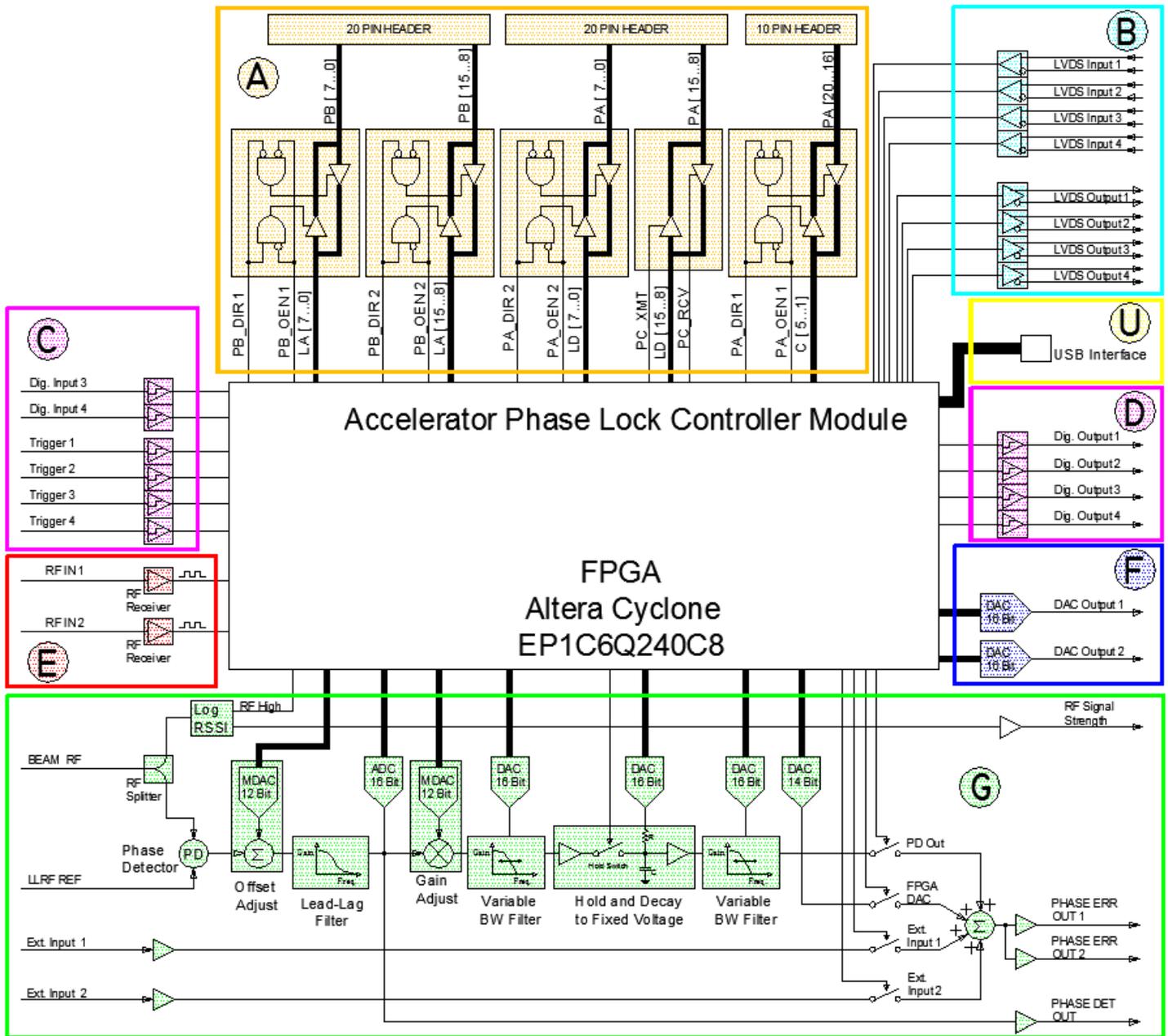


Figure II.1.1 Acceleration Phase Lock Controller block diagram.

- A** The module provides a parallel data bus for an external or daughter module. There are 37 bidirectional lines in 4 groups of 8 and 1 group of 5. This interface is handy for bringing digital data words out to a logic analyzer or oscilloscope.
- B** The module provides a 4 input, 4 output high speed serial interface. These differential LVDS signals connect using compact Harting connectors used on Booster and RF Group VXI Modules. This interface will eventually provide an interface to ACNET through a Booster VXI Module and / or provide a data path for phase control applications running on the larger VXI module.
- C** There are 8 digital inputs to the module. The inputs can provide a digital status or trigger inputs. Each of these can be pulled up through 10k Ohms or pulled down (terminating) through 50 Ohms. The two additional digital inputs (Dig. Input 1 and Dig. Input 2) that can be brought out to the front or rear panel of the module.
- D** There are 4 digital outputs. These outputs are each driven with a 50 Ohm driver (N74F3037D).
- E** There are 2 high speed comparator inputs for converting arbitrary amplitude sinusoidal RF signals into logic level clocks that can be processed with the FPGA.
- F** There are 2 digital to analog converters for observing low frequency phase measurements and other control function variables. The DAC's are 16 bit with a 1.6 micro second update rate.
- G** Section G is the signal path between the phase detector and the control feedback output. The phase detection is followed by a lead-lag filter and two voltage-variable low pass filters. The final stage is a summing amplifier which can select from the filtered phase detector signal, a DAC signal that can provide an adjustable offset or digital control derived by the FPGA, and two buffered external inputs. A more detailed description of this section follows below.
- U** There is a USB interface that is used to manipulate a set of 16, 16 bit parameters. These parameters are used to set scale factors and offsets, time delays and different control and diagnostic modes. A simple protocol has been set up to pass data and implemented in the FPGA, and a MS Windows dialog box type program has been written for the PC side. The FTDI USB chip drivers for Windows and Linux are currently well supported.

II.2 The Analog Signal Path

Section G in the module block diagram is the signal path between the RF inputs and the phase error control feedback output of the module. This section will break down this path and describe the circuit details.

II.2.1 The Phase Detector and Control Loop Filter

The two RF inputs to the phase detector are the Low Level RF (Delayed VCO) and the Booster beam pick signal RF. The phase between these two signals is measured using an Analog Devices AD8302 RF IC. The AD8302 has been characterized in [1]. Figure II.2.1.1 below is a block diagram of the AD8302. Figure II.2.1.2 is the phase difference in degrees to the output in Volts for the AD8302 the following op-amps that provide offset and scaling. The schematic of the phase detector and the lead-lag control loop filter are shown in Figure II.2.1.3.

The phase difference signal has a user settable offset and gain adjustment through the USB interface. The parameters for this are given in a table in a later section. An analog to digital converter running at 5 MHz and digitizing to 16 bits.

FUNCTIONAL BLOCK DIAGRAM

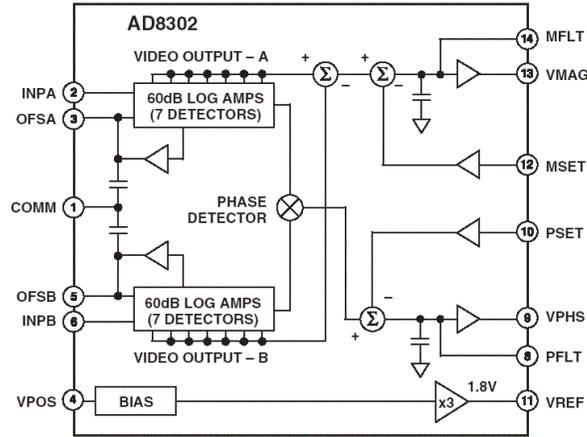
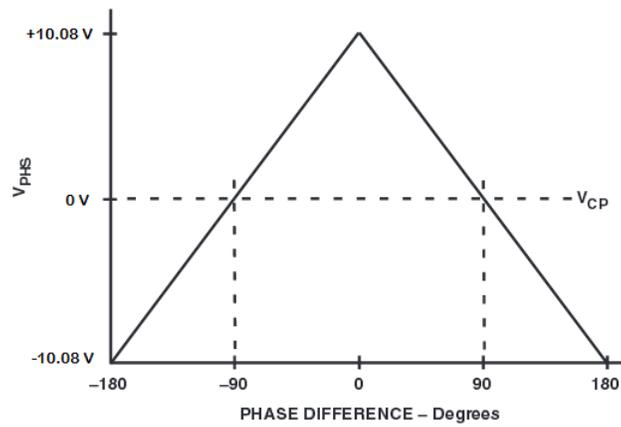
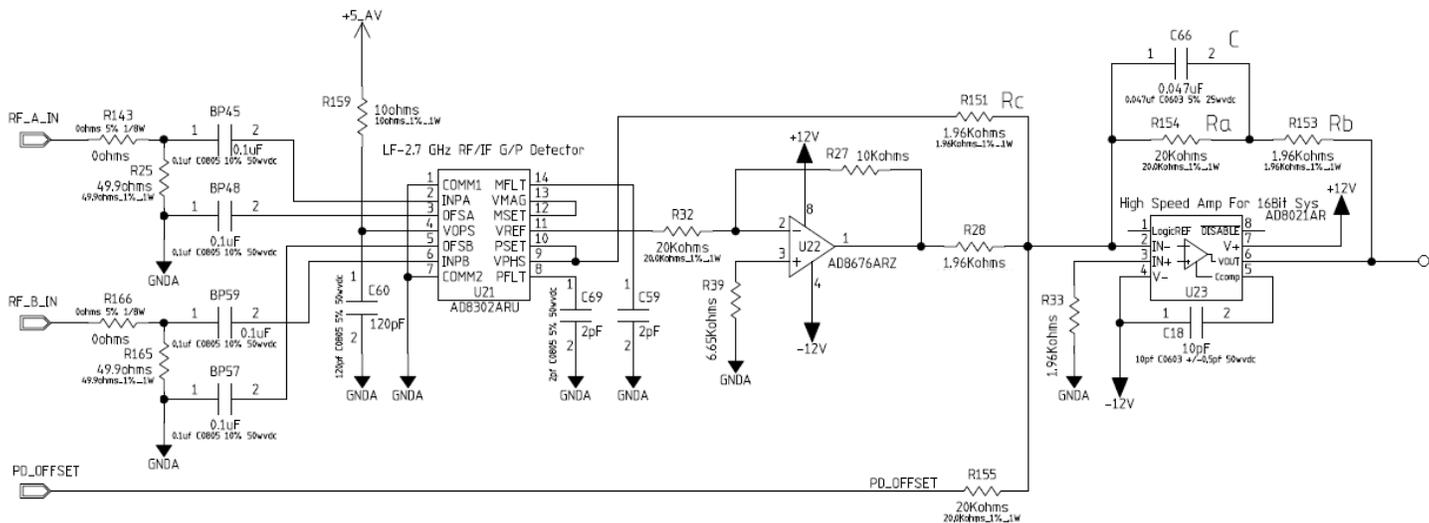


Figure II.2.1.1 Block diagram of the AD8302



Idealized Transfer Characteristics for the Phase Measurement

Figure II.2.1.2 Phase to Voltage output of the AD8302 with added offset and scaling.



Lead-Lag Filter

$$V_{out}/V_{in} = (-1) \left[(s R_a R_b C) + (R_a + R_b) \right] / (s R_a R_c C + R_c)$$

$$\text{Pole} = 1 / (R_a C)$$

$$\text{Zero} = 1 / (R_a C) + 1 / (R_b C)$$

Figure II.2.1.3 The phase detector and the lead-lag control loop filter

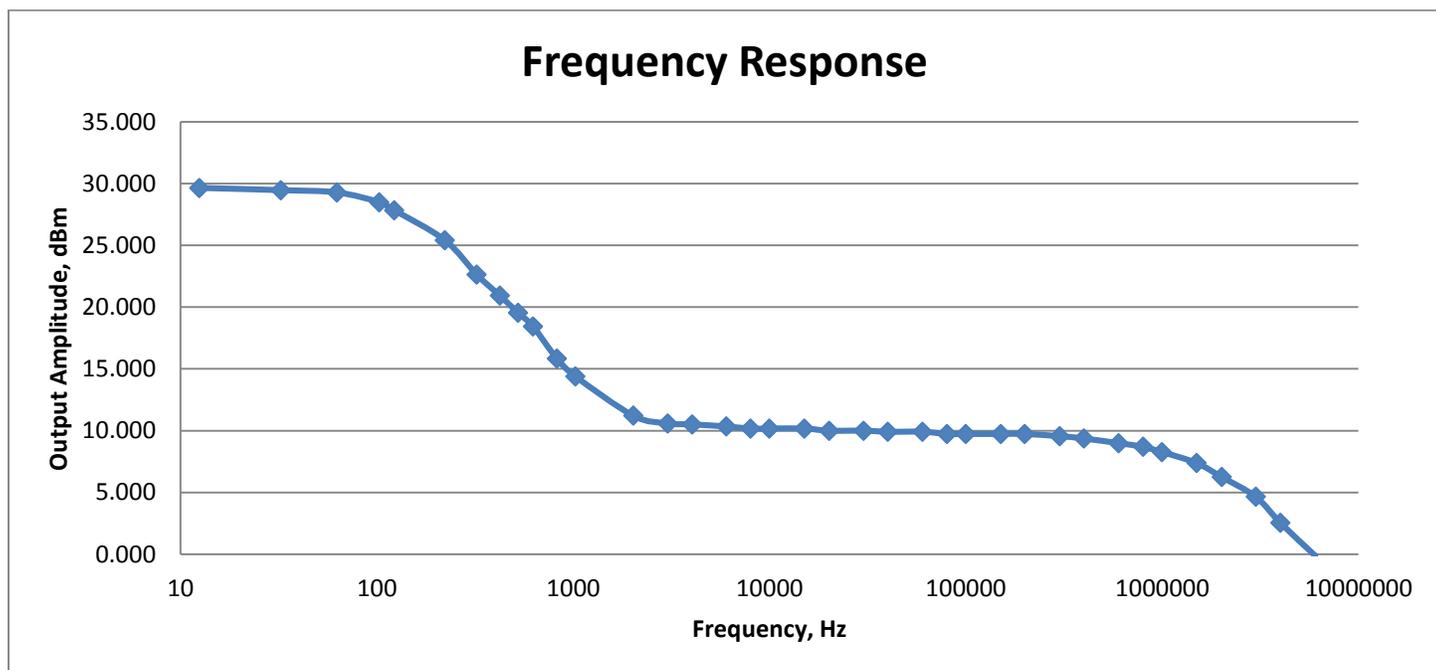


Figure II.2.1.4 Frequency response of the phase detector and loop filter.

II.2.2 The Voltage Variable Bandwidth Filters and Hold Switch

The phase difference signal passes through the voltage variable low pass filters before being driven as the feedback output. During the first part of the Booster cycle these low pass filters have a wide bandwidth (> 1 MHz) and the phase difference passes through unchanged. Approximately 3 ms before the end of the Booster cycle, and beam extraction, the phase difference signal must be held so the Main Injector phase lock controller can take over. As mentioned, small phase oscillations in the Booster beam can result in the Acceleration phase error feedback being held at a high point or low point of the oscillation. The Booster beam has been shown to have larger oscillation if the Acceleration phase error is held at a point other than the mean of the signal. Once the Main Injector phase lock controller has signaled that it is starting the MI phase lock process the two filters are used to decrease the bandwidth of the signal below the frequency of the small beam phase oscillation. The signal settles to its mean, lower frequency value, and the sample and hold switch then holds the Acceleration phase error feedback at this voltage. The second variable filter is used to filter a small charge injection glitch from the switching of the sample and hold. This filter turns on briefly for this purpose.

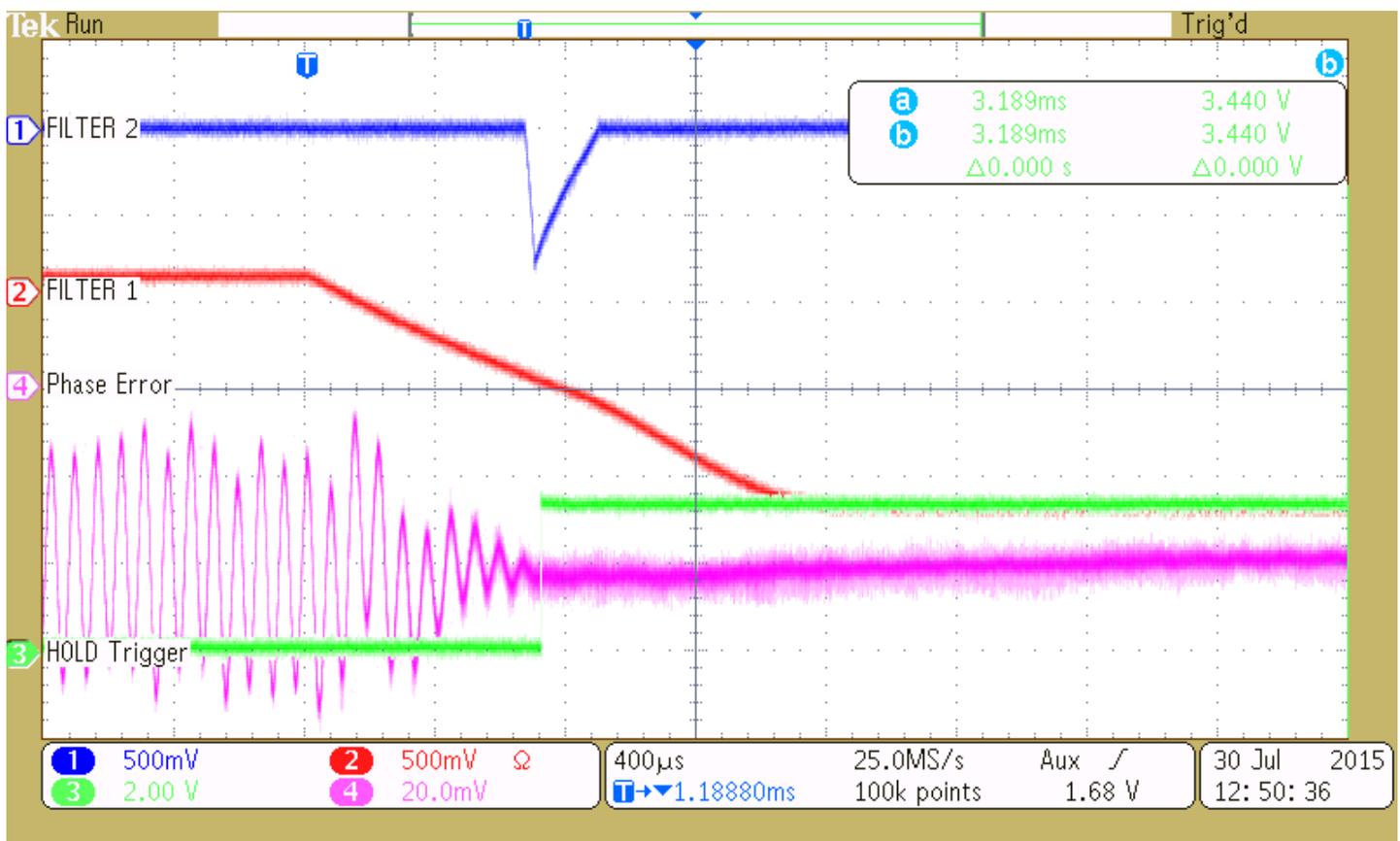


Figure II.2.2.1 Scope picture of the filter and hold process.

The sample and hold switch is also designed such that when it switches to hold the phase error feedback it allows the signal to also decay, with an RC time constant, to a settable final voltage.

The figures below are the schematic of one of the filters and an explanation of the Sallen-Key filter.

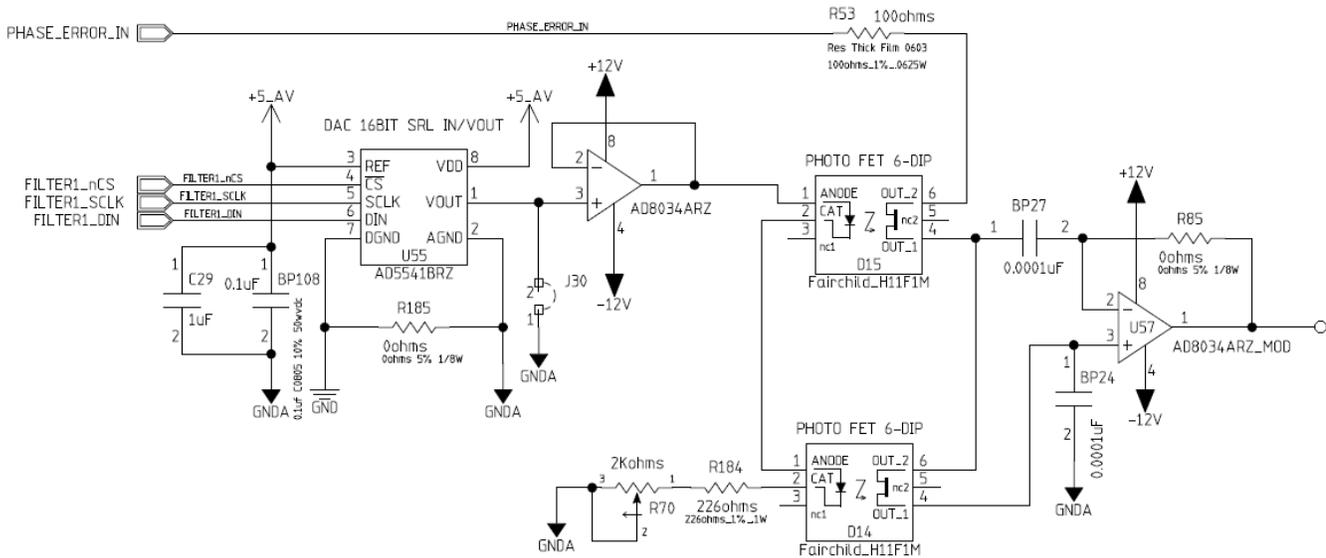


Figure II.2.2.2 Schematic of one of the voltage variable bandwidth filters.

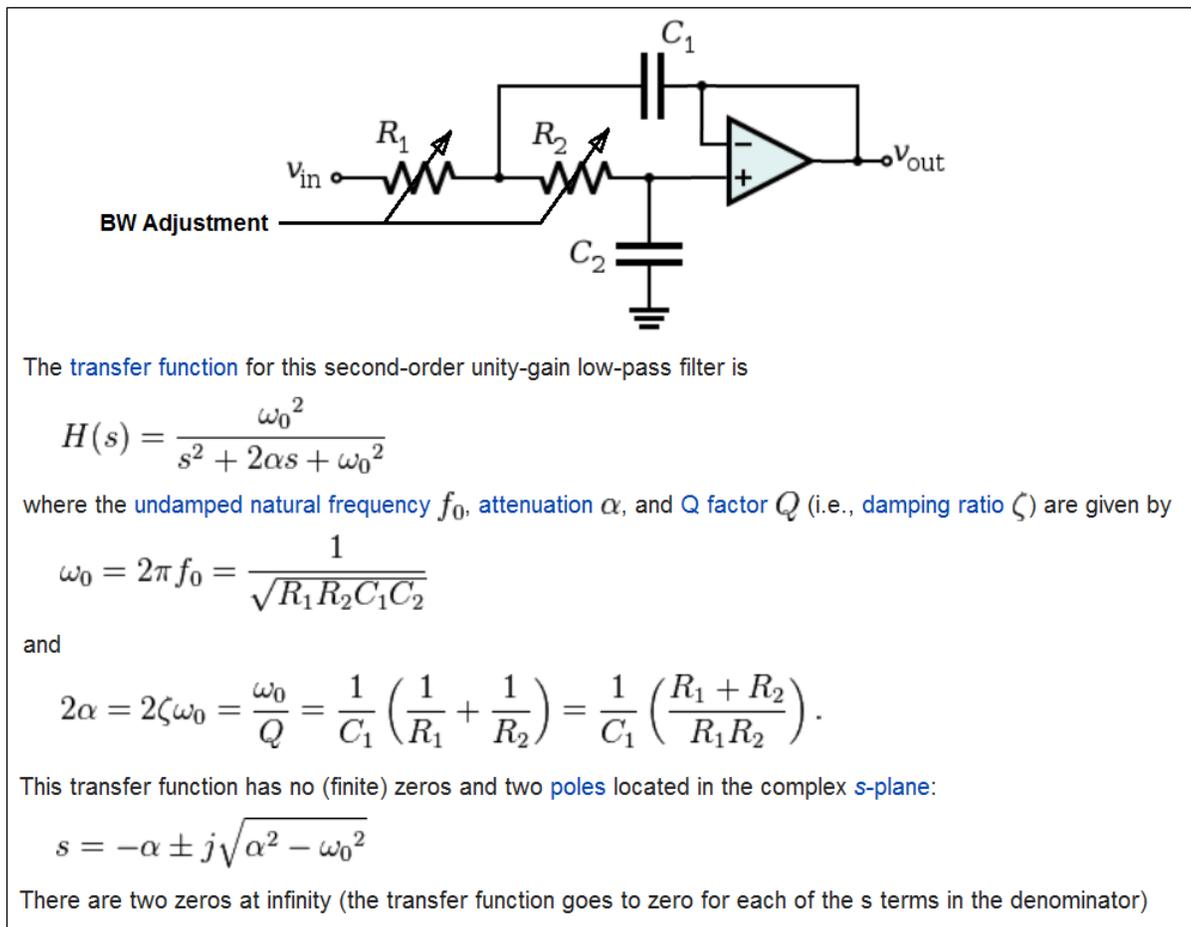


Figure II.2.2.3 Description of the Sallen-Key filter (Wikipedia)

Default Outputs

```

Module_Switch_Sel <= '1'
Extern_Switch_Sel <= '0'
Filter_1_Trigger <= '0'
Filter_2_Trigger <= '0'
HOLD_Trigger <= '0'

```

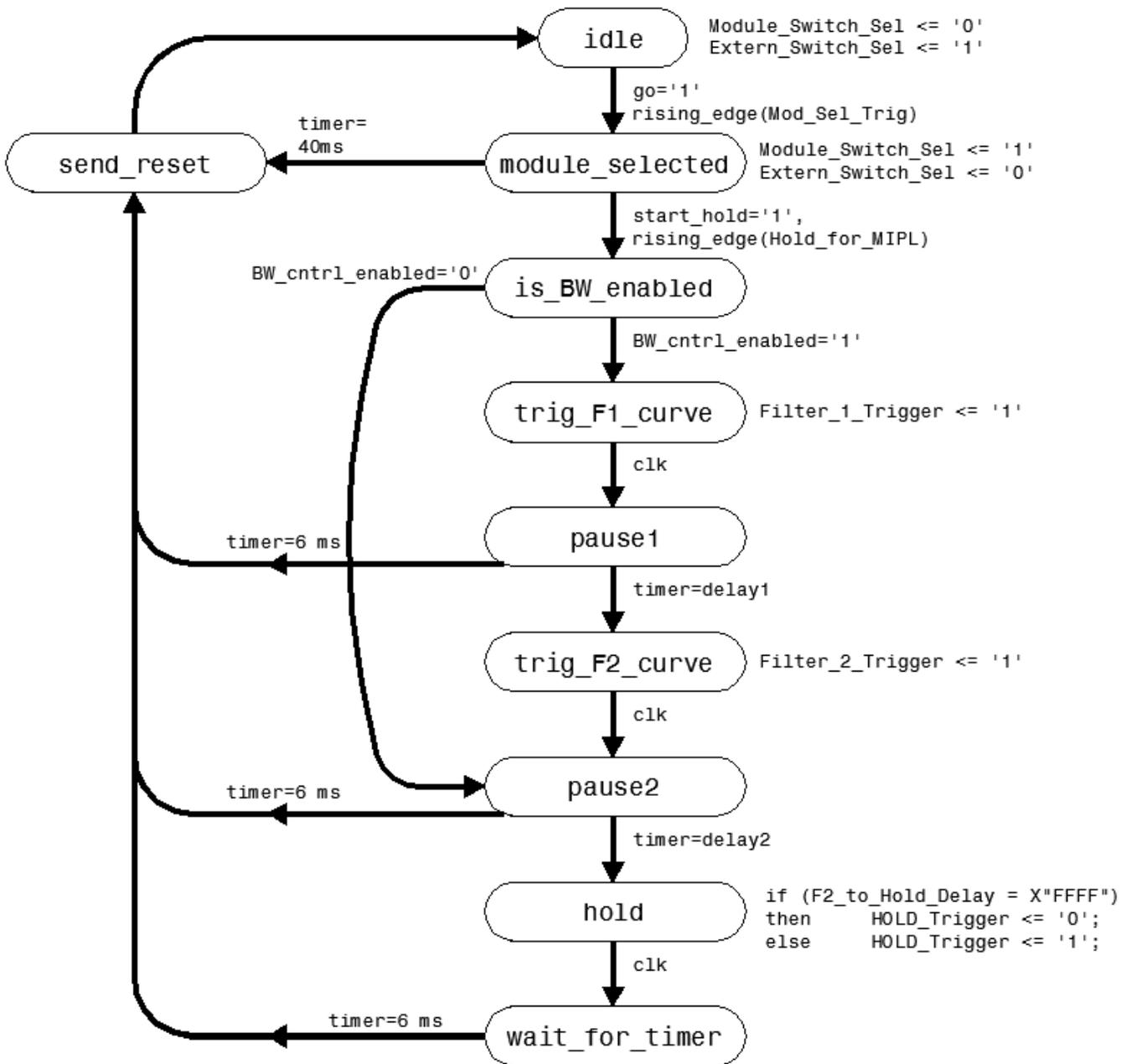


Figure II.2.2.4 Filter Sequence logic diagram.

III. Settable Parameters and Their Function

The module has a USB interface through which several parameters of the module can be set. The USB interface is implemented using an FTDI UM245R USB Parallel FIFO Development Module. The Microsoft Windows driver is well supported and a dialog box style windows program has been written to manage as many as 16 parameter setting. After

settings have been made the parameters can be saved to EEPROM memory and reloaded on power up by momentarily pressing the Save\Rst button on the modules front panel.

A protocol has been written to utilize the 8 bit FIFO output of the UM245R interface [2]. A portion of this protocol was implemented in the modules FPGA to manage the 16 bit parameter values. Table III.1 lists the Accelerator phase controller's settable parameters as implemented in the current version of the FPGA project folder "phasedet3 -- 150813_ACCEL_First Field Version"

Table III.1 Acceleration Phase Controller (ACCEL PD ver. 3) USB settable parameters.

Param #	Typical Value	Number Format	Name	Description
0	0x0500	12 bit OB	PD Gain	Phase Detector Gain adjustment. 12 bit OB
1	0x0800	12 bit OB	PD Offset	Phase Detector Offset adjustment. 12 bit OB
2	0x4C00	16 bit OB	Hold_Offset	This is the value the output decays to after activating the Hold Switch. 16 bit OB with voltage ranges from - 2.5 V to +7.5 V
3	0X2000	16 bit uint	F1_Final_Pt	Final point of Filter 1's BW curve. 16 bit unsigned int.
4	0X0040	16 bit uint	F1_Intv_Clks	Curve time scaling factor for Filter 1. Number of 12.5 ns clocks between curve sample updates. Full curve has 1024 points. 16 bit unsigned int.
5	0X0000	16 bit uint	F2_Final_Pt	Final/Lowest point of Filter 2's BW curve. 16 bit unsigned int.
6	0X0010	16 bit uint	F2_Intv_Clks	Curve time scaling factor for Filter 2. Number of 12.5 ns clocks between curve sample updates. Full curve has 1024 points. 16 bit unsigned int.
7	0X7800	16 bit uint	F1_F2_Delay	Delay between when the Filter 1 Curve starts and when the Filter 2 Curve starts. Number of 12.5 ns clocks. 16 bit unsigned int.
8	0XB000	16 bit uint	F2_Hold_Delay	Delay between when the Filter 2 Curve starts and when the Hold switch is activated. Number of 12.5 ns clocks. 16 bit unsigned int.
9	0X1A78	14 bit OB	FPGA_DAC DPOT_Cntrl	This sets the value of the FPGA DAC which acts as a fixed output offset. 14 bit OB (0x2000 = zero). <i>*This is used to adjust offset out of the External Input</i> Alternately, this register acts as the control word for adjusting digital potentiometers on the board. (see DPOT Control Word definition below)
10	0X8000	16 bit	DAC_TEST	Register used for Testing the Auxiliary front panel DAC's and the Filter Curve DAC's. 16 bit.
11	0X0244	--	CNTRL_REG	This is the diagnostic control register (see Diagnostics Section)

IV Modules IO Connections

Table IV.1 Module Front IO connections

Label	Description
Front of Module	
T1	Acceleration Gate Input (Beam Gate AND Accel Gate): This input is not currently applied in the logic.
T2	Module Select Trigger: If Mod_Sel_Trig fires, the phase detector control signal generated by this module is routed to the output and a timer will time the cycle and send a cycle reset signal at the end. If the Mod_Sel_Trig does not fire at the beginning of the cycle, the External 1 input is routed to the output and this module remains inactive.
T3	MI Phase Lock Trigger (i.e. Hold for MIPL) : This triggers the BW control and output hold process.
T4	Enable Bandwidth Control: The bandwidth control process is enabled when this input is High, or simply not pulled down with a 50 Ohm terminator.
DI3	Enable Filter 2: This signal is AND'd with the Filter_2_Trigger output of the Sequence Controller that starts the bandwidth narrowing curve for Filter 2.
DI4	No current use
DO3	Beam RF Present (diagnostic): RSSI measurement of the RF A input.
DO4	HOLD_PD_1 (diagnostic): Internally generated output hold signal set in response to the MI Phase Lock Trigger.
DAC 1	See Diagnostics Section
DAC 2	See Diagnostics Section
RF IN 1	High speed comparator input with LVDS output connected to FPGA.
RF IN 2	High speed comparator input with LVDS output connected to FPGA.

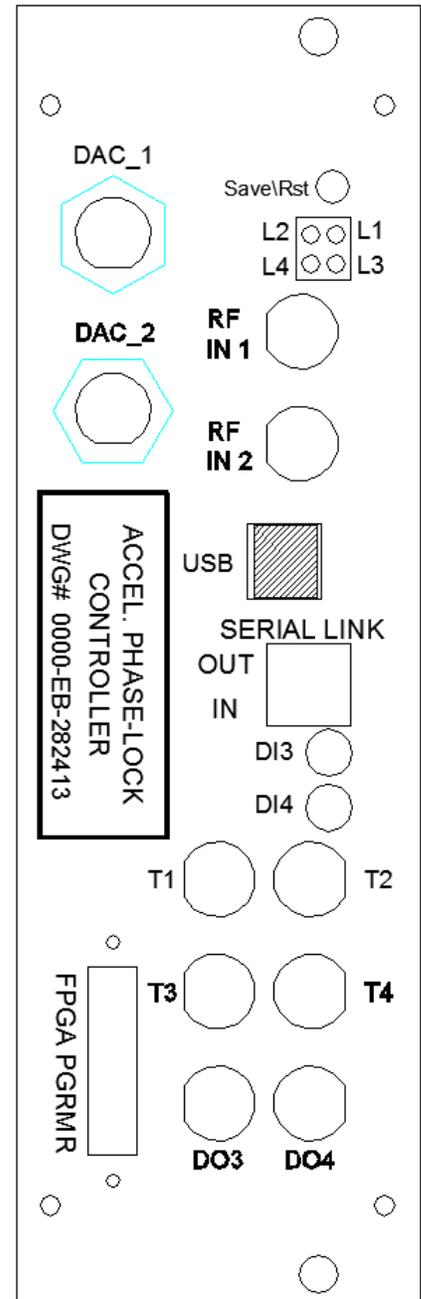
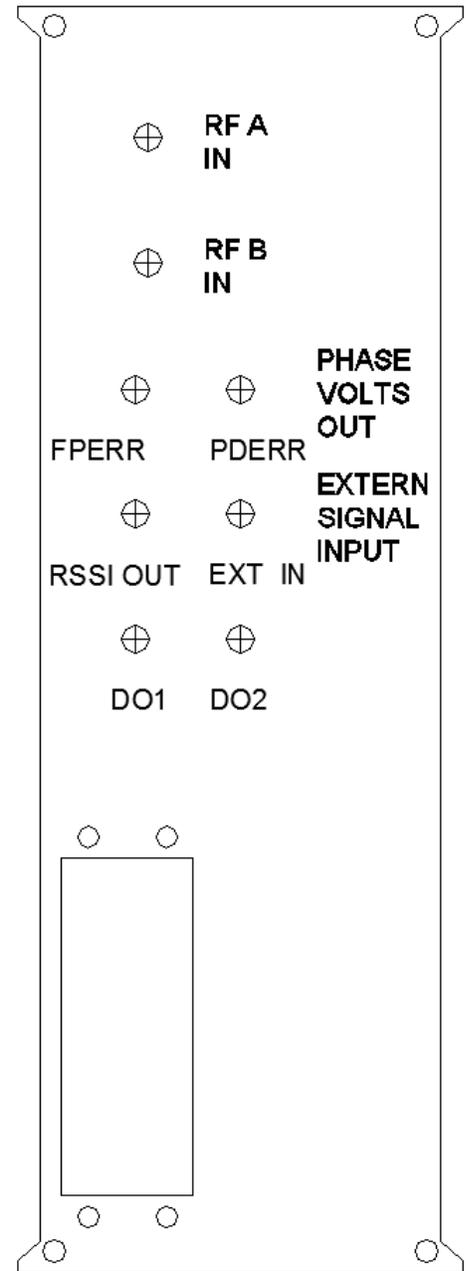


Table IV.2 Module Rear IO connections

Label	Description
Rear of Module	
RF A IN	Input A to the phase detector and input to the RSSI.
RF B IN	Input B to the phase detector.
FPERR	Direct output of the phase detector before gain scaling
PDERR	Phase Detector output after gain scaling and BW control.
RSSI OUT	Received Signal Strength voltage for the RF A Input
EXT IN	External Input that can be switched on in place of the phase detector output or summed with the phase detector output. Use for multiplexing between systems.
DO 1	Copy of the Acceleration Beam Gate (diagnostic)
DO 2	RF Present Output (diagnostic)



V Diagnostics

Table V.1 Test Interface selection of different IO options using Parameter 11.

Bits	Description	
[3..0]	<p>Selects the signal to output through the auxiliary DAC 1 output.</p> <p>Aux DACs have an offset binary coding: 0x0000 = -10V 0x8000 = 0V 0xFFFF = +10V</p>	<p>[0,0,0,0] => Filter 1 BW Control Curve</p> <p>[0,0,0,1] => Filter 2 BW Control Curve</p> <p>[0,0,1,0] => DAC Test set by Parameter 10</p> <p>[0,0,1,1] => FPERR digitized phase detector output ADC1</p> <p>[0,1,0,0] => FPERR digitized phase detector output ADC1</p> <p>All Others => reserved</p>
[7..4]	<p>Selects the signal to output through the auxiliary DAC 2 output.</p> <p>Aux DACs have an offset binary coding: 0x0000 = -10V 0x8000 = 0V 0xFFFF = +10V</p>	<p>[0,0,0,0] => Filter 1 BW Control Curve</p> <p>[0,0,0,1] => Filter 2 BW Control Curve</p> <p>[0,0,1,0] => DAC Test set by Parameter 10</p> <p>[0,0,1,1] => FPERR digitized phase detector output ADC1</p> <p>[0,1,0,0] => FPERR digitized phase detector output ADC1</p> <p>All Others => reserved</p>
[11..8]	<p>Selects a 16 bit word to send to the logic analyzer connections at J14</p>	<p>See Table V.2 for Logic Analyzer connection pinout.</p> <p>[0,0,0,0] => output disabled.</p> <p>[0,0,0,1] => FPERR digitized phase detector output ADC1</p> <p>[0,0,1,0] => FPERR digitized phase detector output ADC1</p> <p>[0,0,1,1] => Filter 1 BW Control Curve</p> <p>[0,1,0,0] => Filter 2 BW Control Curve</p> <p>[0,1,0,1] => Bit Status Register. See Figure V.1</p> <p>All Others => reserved</p>
[12]	Production Test Mode	Used in module test only
[13]	Use Alternate Digital Output Assignments	This selects the alternate set of digital output assignments. Used for diagnostics only.
[15..14]	reserved	

Table VII.4 External Bus and Diagnostics Logic Analyzer bits out.

Generic Schematic Name	Current Signal Name	Connection	Function
PB[0]	ADDR[0]	J13-19	Address Bus
PB[1]	ADDR[1]	J13-18	
PB[2]	ADDR[2]	J13-17	
PB[3]	ADDR[3]	J13-16	
PB[4]	ADDR[4]	J13-15	
PB[5]	ADDR[5]	J13-14	
PB[6]	ADDR[6]	J13-13	
PB[7]	ADDR[7]	J13-12	
PB[8]	ADDR[8]	J13-11	
PB[9]	ADDR[9]	J13-10	
PB[10]	ADDR[10]	J13-9	
PB[11]	ADDR[11]	J13-8	
PB[12]	ADDR[12]	J13-7	
PB[13]	ADDR[13]	J13-6	
PB[14]	ADDR[14]	J13-5	
PB[15]	ADDR[15]	J13-4	
PA[0]	DATA[0]	J14-19	Data Bus / Diagnostics Logic Analyzer Mux'ed Data Out
PA[1]	DATA[1]	J14-18	
PA[2]	DATA[2]	J14-17	
PA[3]	DATA[3]	J14-16	
PA[4]	DATA[4]	J14-15	
PA[5]	DATA[5]	J14-14	
PA[6]	DATA[6]	J14-13	
PA[7]	DATA[7]	J14-12	
PA[8]	DATA[8]	J14-11	
PA[9]	DATA[9]	J14-10	
PA[10]	DATA[10]	J14-9	
PA[11]	DATA[11]	J14-8	
PA[12]	DATA[12]	J14-7	
PA[13]	DATA[13]	J14-6	
PA[14]	DATA[14]	J14-5	
PA[15]	DATA[15]	J14-4	
CNTRL[1]	EXT_Rd_Out	J15-9	Read Pulse
CNTRL[2]	EXT_Wr_Out	J15-7	Write Pulse / Diagnostics Logic Analyzer Data Strobe
CNTRL[3]	EXT_CS1_Out	J15-5	Chip Select
CNTRL[4]	EXT_CS2_Out	J15-3	Chips Select
CNTRL[5]	reserved	J13-3, J14-3	

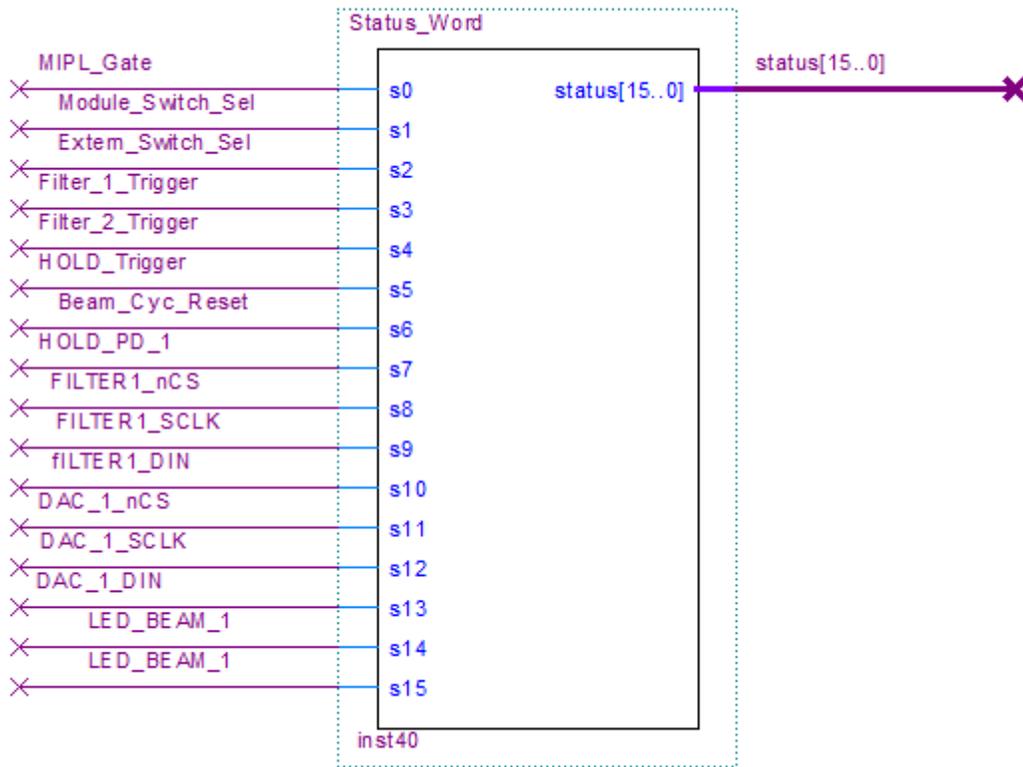


Figure V.1 Bit Status Register

VI Calibrations

Table III.1 Acceleration Phase Controller (ACCEL PD ver. 3) USB settable parameters.

Param #	Typical Value	Number Format	Name	Description
0	0x0500	12 bit OB	PD Gain	Phase Detector Gain adjustment. 12 bit OB
1	0x0800	12 bit OB	PD Offset	Phase Detector Offset adjustment. 12 bit OB
2	0x4C00	16 bit OB	Hold_Offset	This is the value the output decays to after activating the Hold Switch. 16 bit OB with voltage ranges from -2.5 V to +7.5 V
3	0X2000	16 bit uint	F1_Final_Pt	Final point of Filter 1's BW curve. 16 bit unsigned int.
4	0X0040	16 bit uint	F1_Intv_Clks	Curve time scaling factor for Filter 1. Number of 12.5 ns clocks between curve sample updates. Full curve has 1024 points. 16 bit unsigned int.
5	0X0000	16 bit uint	F2_Final_Pt	Final/Lowest point of Filter 2's BW curve. 16 bit unsigned int.
6	0X0010	16 bit uint	F2_Intv_Clks	Curve time scaling factor for Filter 2. Number of 12.5 ns clocks between curve sample updates. Full curve has 1024 points. 16 bit unsigned int.
7	0X7800	16 bit uint	F1_F2_Delay	Delay between when the Filter 1 Curve starts and when the Filter 2 Curve starts. Number of 12.5 ns clocks. 16 bit unsigned int.
8	0XB000	16 bit uint	F2_Hold_Delay	Delay between when the Filter 2 Curve starts and when the Hold switch is activated. Number of 12.5 ns clocks. 16 bit unsigned int.
9	0X1A82	14 bit OB	FPGA_DAC DPOT_Cntrl	This sets the value of the FPGA DAC which acts as a fixed output offset. 14 bit OB (0x2000 = zero). Alternately, this register acts as the control word for adjusting digital potentiometers on the board. (see DPOT Control Section)
10	0X8000	16 bit	DAC_TEST	Register used for Testing the Auxiliary front panel DAC's and the Filter Curve DAC's. 16 bit.
11	0X0244	--	CNTRL_REG	This is the diagnostic control register (see Diagnostics Section)

References

- [1] C. Drennan, "Characterization of the Fast Phase Detector in the Booster Low Level RF System", March 2003, Internal Document "Beams-doc-3367-v1" at <http://beamdocs.fnal.gov>.
- [2] C. Drennan, "Data Transfer Protocol for the USB to FIFO Interface", May 2010, Internal Document "Beams-doc-4884-v1" at <http://beamdocs.fnal.gov>.