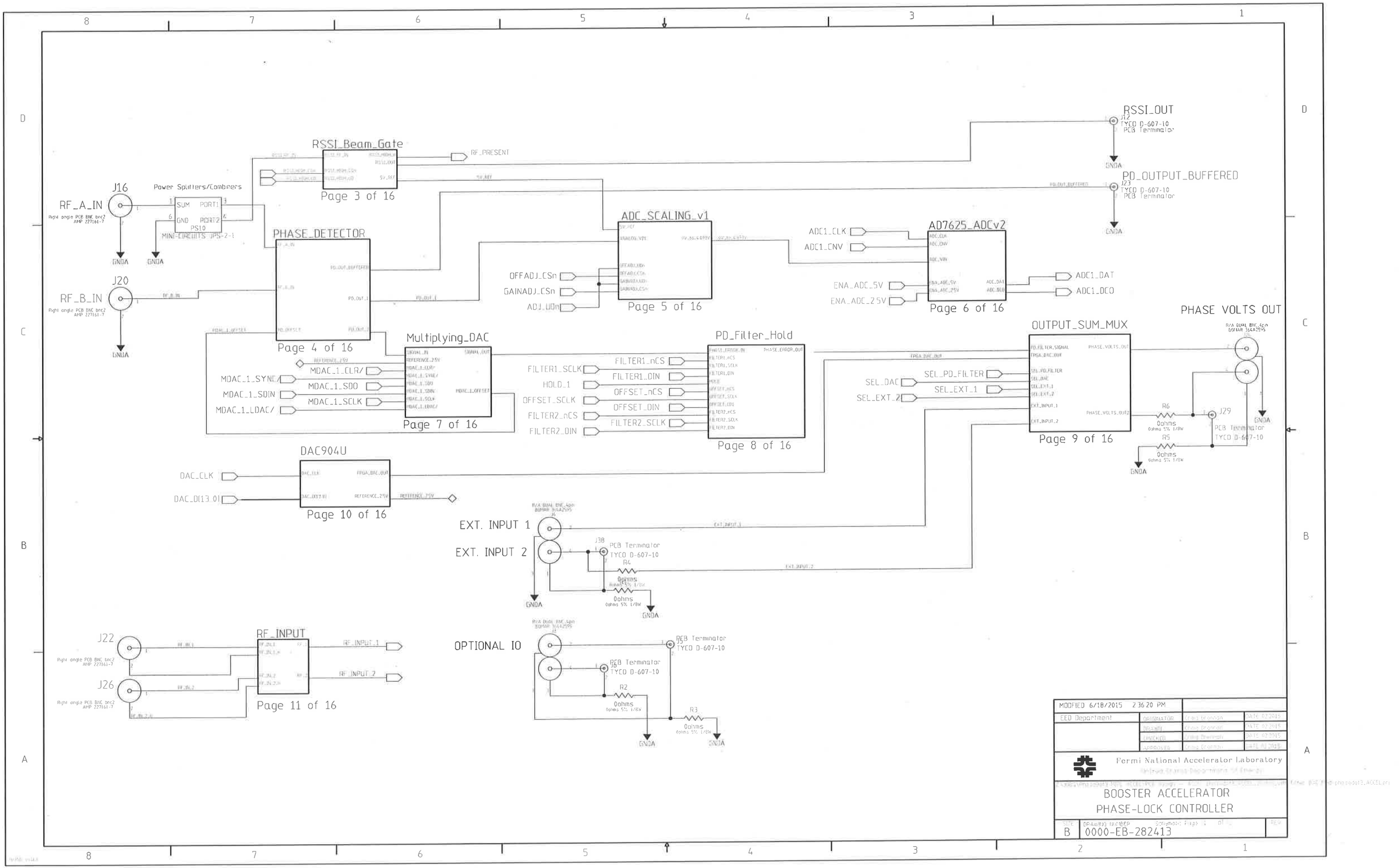

MODIFIED 6/18/2015 2:36:20 PM			
EED Department	ORIGINATOR	Hanz Cheung	DATE 02/2015
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BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	REV
B	0000-EB-282413	

POWER_REGULATORS

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FPGA_MEMORY

DIN_1
DIN_2
DIN_3
DIN_4
TRIG_4
TRIG_3
TRIG_2
TRIG_1
DATA_LINK_IN1
DATA_LINK_IN2
DATA_LINK_IN3
DATA_LINK_IN4
USB_RXE_n
USB_TXE_n
DIG_OUT_1
DIG_OUT_2
DIG_OUT_3
DIG_OUT_4
LED1
LED2
LED3
LED4
DATA_LINK_OUT1
DATA_LINK_OUT2
DATA_LINK_OUT3
DATA_LINK_OUT4
USB_RD_n
USB_WR_n
DAC_CLK
DAC_DI[13..0]
MDAC_1_CLR/
MDAC_1_SYNC/
MDAC_1_SDO
MDAC_1_SDIN
MDAC_1_SCLK
MDAC_1_LDAC/
DAC_1_DIN
DAC_1_SCLK
DAC_1_nCS
DAC_2_DIN
DAC_2_SCLK
DAC_2_nCS
PA[20..0]
PB[15..0]
SEL_PD_FILTER
SEL_EXT_1
SEL_EXT_2
SEL_DAC
HOLD_1
FILTER1_nCS
FILTER1_SCLK
FILTER1_DIN
OFFSET_nCS
OFFSET_SCLK
OFFSET_DIN
FILTER2_nCS
FILTER2_SCLK
FILTER2_DIN
ADC1_CLK
ADC1_CNV
ENA_ADC_5V
ENA_ADC_2.5V
RSSI_HIGH_CSn
RSSI_HIGH_UD
DPOT_U_nD
DAC_1_GAIN_nCS
DAC_1_OFFS_nCS
DAC_2_OFFS_nCS
DAC_2_GAIN_nCS
ADJ_UDn
OFFADJ_CSn
GAINADJ_CSn
ADC1_DAT
ADC1_DCO
RF_INPUT_1
RF_INPUT_2
RF_PRESENT
PB_SW
ENCODER1_A
ENCODER1_B
SW_BIT4
SW_BIT3
SW_BIT2
SW_BIT1

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POWER_REGULATORS

+3.3V
R14
10Kohms
SPST Push Button Right Angle
PB_SW
SW10
ALCO TSP05TD11CGRA0
GND

Incremental_Encoder
Bourns 3315Y-025-016L
+3.3V
R206
10Kohms
R208
10Kohms
U76
GND

+3.3V
R214
10Kohms
R207
10Kohms
R211
10Kohms
R213
10Kohms
FRONKRIEP-S
NKK FRONKRIEP-S
SW1
16 Pos ROTARY DIP
GND

+3.3V
BP98
0.1uF
BP107
0.1uF
C90
10uF
GND

+3.3V
USB_RD_n
USB_WR_n
USB_D[7..0]
U56
CY7C68013A-56LTXC
USB_RXE_n
USB_TXE_n
GND

DIGITAL_IO_BUFFERS

J42
TYCO_D-607-10
PCB Terminator
J45
LEMO_5pin_DA
LEMO EPL.00.250.NTN
J8
LEMO_5pin_DA
LEMO EPL.00.250.NTN
GND

TRIG_1
TRIG_2
TRIG_3
TRIG_4
DIN_1
DIN_2
DIN_3
DIN_4
LED1
LED2
LED3
LED4
DIG_OUT_1
DIG_OUT_2
DIG_OUT_3
DIG_OUT_4

+5V
D16
R123
226ohms
DIALIGHT 553-0122 Green
D15
R122
226ohms
DIALIGHT 553-0122 Green
D17
R125
226ohms
DIALIGHT 553-0122 Green
D17
R124
226ohms
DIALIGHT 553-0122 Green

J51
TYCO_D-607-10
PCB Terminator
J54
R27
0ohms
R8
0ohms
J57
J60
R9
0ohms
R226 8W
0ohms

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AUX_DACs

DAC_1_nCS
DAC_1_SCLK
DAC_1_DIN
DAC_2_nCS
DAC_2_SCLK
DAC_2_DIN
DPOT_U_nD
DAC_1_GAIN_nCS
DAC_1_OFFS_nCS
DAC_2_OFFS_nCS
DAC_2_GAIN_nCS
DAC_1_OUTPUT
DAC_2_OUTPUT

R93
0ohms
J40
PCB Terminator
TYCO D-607-10
GNDA

DAC 1 VOLTS OUT

R107
0ohms
J46
PCB Terminator
TYCO D-607-10
GNDA

DAC 2 VOLTS OUT

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FRONT_PANEL_LVDS_IN[4..1]

HARTING 27 21 121 8000
LVDS_IN_1n
LVDS_IN_1p
LVDS_IN_2n
LVDS_IN_2p
LVDS_IN_3n
LVDS_IN_3p
LVDS_IN_4n
LVDS_IN_4p
J11
GND

LVDS_FP_INTERFACE

LVDS_IN_1n
LVDS_IN_1p
LVDS_IN_2n
LVDS_IN_2p
LVDS_IN_3n
LVDS_IN_3p
LVDS_IN_4n
LVDS_IN_4p
DATA_LINK_OUT1
DATA_LINK_OUT2
DATA_LINK_OUT3
DATA_LINK_OUT4
DATA_LINK_IN1
DATA_LINK_IN2
DATA_LINK_IN3
DATA_LINK_IN4

Page 15 of 16

FRONT_PANEL_LVDS_OUT[4..1]

HARTING 27 21 121 8000
J10
GND

+12V
-12V
+5V
+3.3V
3m2510-6003UB
J15
GNDA
GND

3m2520-6007UB
J14
PA[20..0]
GND

3m2520-6002UB
J13
PB[15..0]
GND

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EED Department	ORIGINATOR	Craig Drennen	DATE 02.2015
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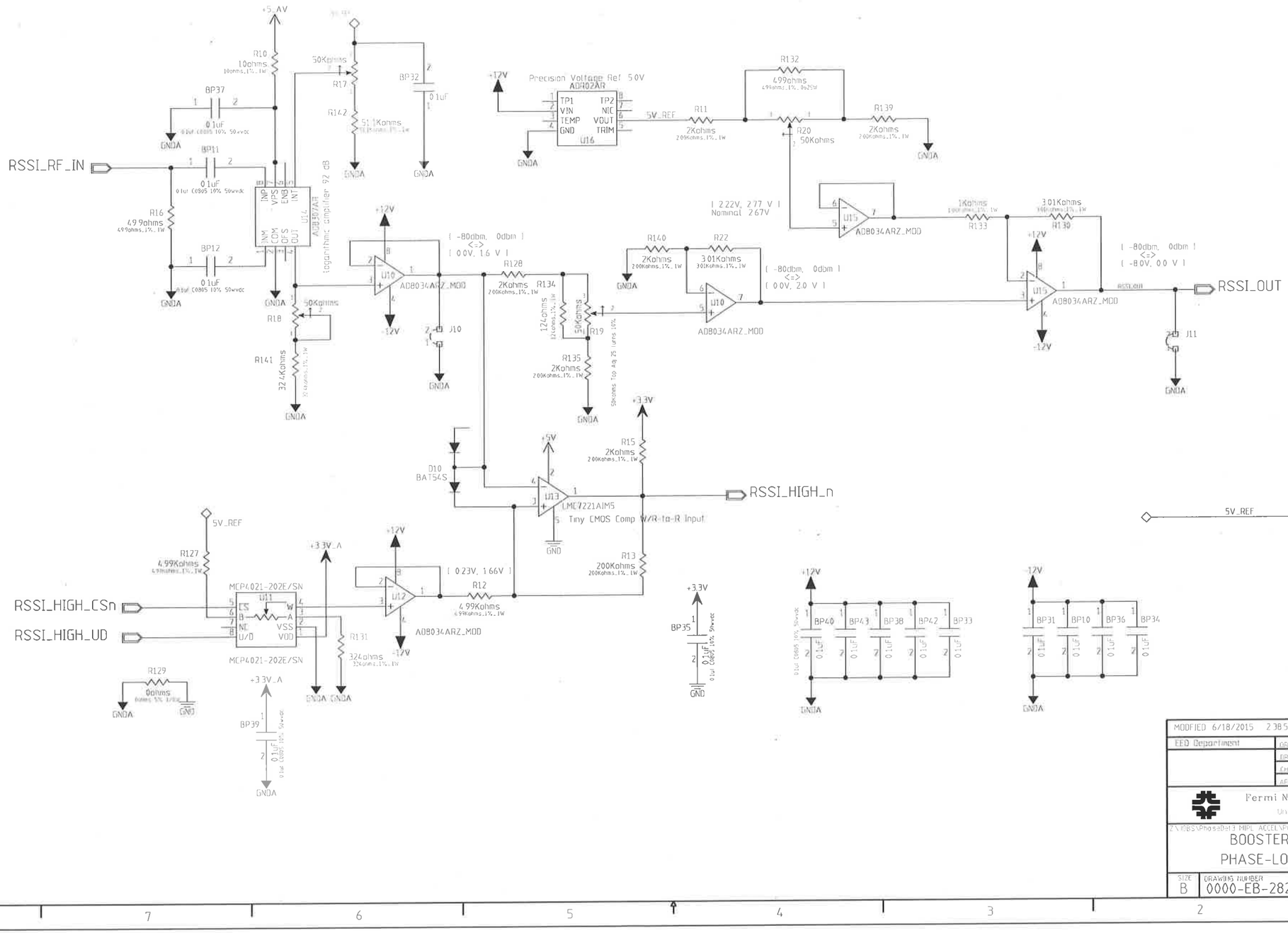
B	0000-EB-282413	

RSSI Beam Gate, page 3 of 16



MODIFIED 6/18/2015 2:38:54 PM			
EEO Department	ORIGINATOR	Craig Drennan	DATE 07/2015
	DRAWN	Craig Drennan	DATE 07/2015
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BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	REV
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Phase Detector, page 4 of 16

Lead-Lag Filter

Vout/Vin = (-1) [(s Ra Rb C) + (Ra + Rb)] / (s Ra Rc C + Rc)

Pole = 1 / (Ra C)

Zero = 1 / (Ra C) + 1 / (Rb C)

ECO: These Resistors Are Not Installed Unless PI Atten. is Applied

+5_AV

C73 0.1uF 10uF BP15

GNDA

R159 10ohms 10ohms,1%,.1W

LF-27 GHz RF/IF G/P Detector

RF_A_IN

R143 0ohms 5% 1/8W

R144 0ohms

R25 49.9ohms 49.9ohms,1%,.1W

BP45 0.1uF C0805 10% 50wvdc

BP48 0.1uF C0805 10% 50wvdc

RF_B_IN

R166 0ohms 5% 1/8W

R168 0ohms

R165 49.9ohms 49.9ohms,1%,.1W

BP59 0.1uF C0805 10% 50wvdc

BP57 0.1uF C0805 10% 50wvdc

U21 AD8302ARU

COMM1 MFLT
INPA VMAG
UrSA MSET
VOPS VREF
OFSB PSET
INPB VPHS
COMM2 PFLT

C60 120pF 120pF C0805 5% 50wvdc

C69 2pF 2pF C0805 5% 50wvdc

C59 2pF 2pF C0805 5% 50wvdc

R32 20Kohms 20.0Kohms,1%,.1W

R39 6.65Kohms 6.65Kohms,1%,.1W

U27 AD8676ARZ 4 Ultraprecision OpAmp

+12V R27 10Kohms 10.0Kohms,1%,.0625W

-12V

R151 Rc 196Kohms 196Kohms,1%,.1W

R28 196Kohms 196Kohms,1%,.1W

PD_OFFSET

R155 20Kohms 20.0Kohms,1%,.1W

-12V BP55 0.1uF C0805 10% 50wvdc

+12V BP52 0.1uF C0805 10% 50wvdc

C66 C 0.047uF 0.047uF C0603 5% 25wvdc

R154 Ra 20Kohms 20.0Kohms,1%,.1W

R153 Rb 196Kohms 196Kohms,1%,.1W

High Speed Amp For 16Bit Sys ADB021AR

U23 logicREF DISABLE IN- IN+ V- V+ Vout Ccomp

R33 196Kohms

C18 10pF 10pF C0603 +/-0.5pf 50wvdc

BP54 0.1uF C0805 10% 50wvdc

C22 10uF 10uF C7343 20% 35wvdc

+12V C19 10uF BP47 0.1uF C0805 10% 50wvdc

PD_OUT_1

R158 PD_OUT_2 0ohms 5% 1/8W

J19

R40 2Kohms 2.00Kohms,1%,.1W

R170 2Kohms 2.00Kohms,1%,.1W

High Speed Amp For 16Bit Sys ADB021AR

U38 logicREF DISABLE IN- IN+ V- V+ Vout Ccomp

R51 1Kohms 1.00Kohms,1%,.1W

PD_OUT_BUFFERED

C21 10pF 10pF C0603 +/-0.5pf 50wvdc

BP67 0.1uF C0805 10% 50wvdc

BP68 0.1uF C0805 10% 50wvdc

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EED Department	ORIGINATOR	Craig Drennon	DATE 02.2015
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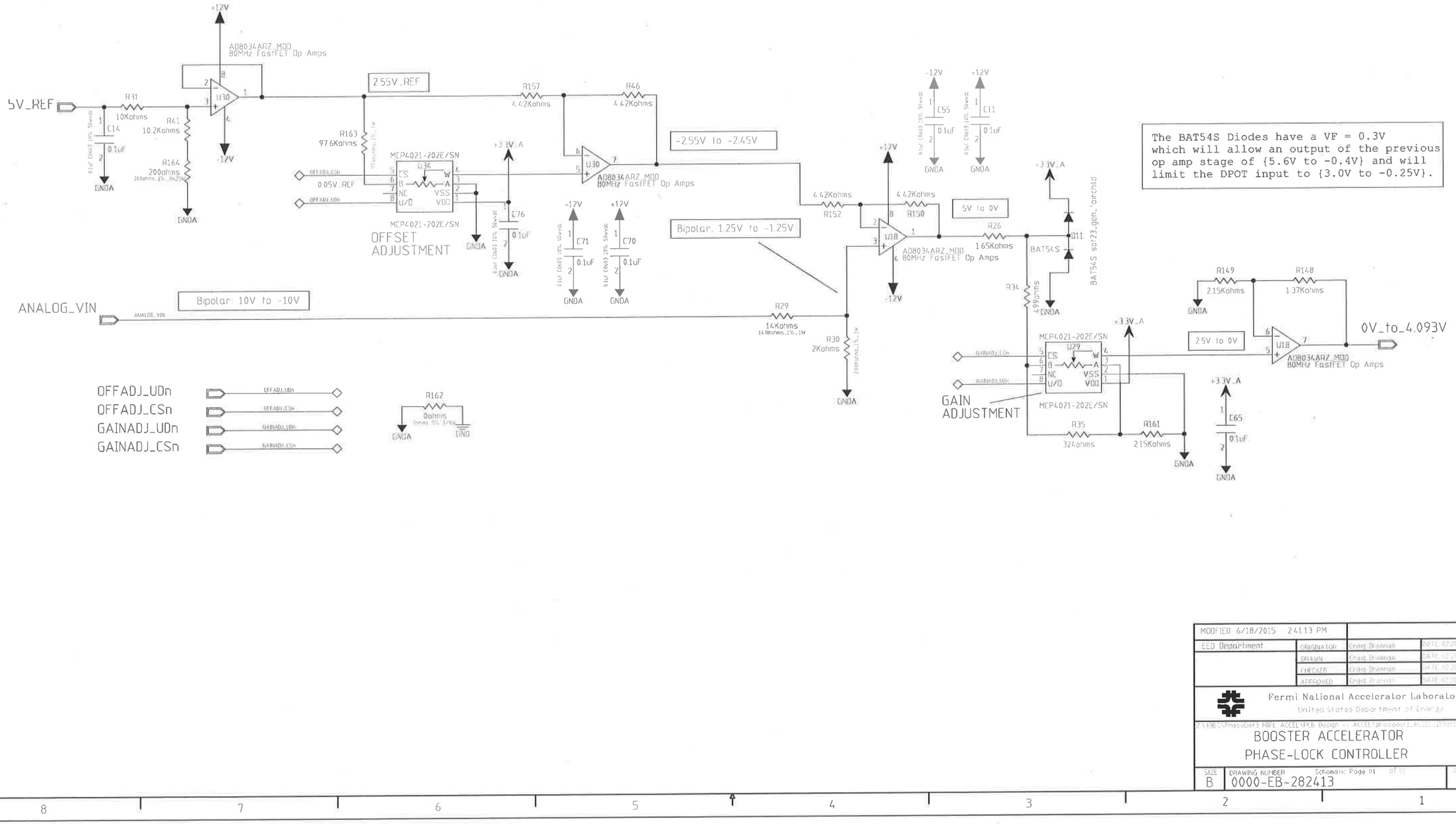
BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	REV
B	0000-EB-282413 Schematic Page 01 of 01	

ADC 1 Scaling, page 5 of 16



MODIFIED 6/18/2015 2:41:13 PM			
EED Department	ORIGINATOR	Craig Drennon	DATE 02.2015
	DRAWN	Craig Drennon	DATE 02.2015
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BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	REV
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AD7625 ADC, page 6 of 16

ADC_VIN
R23 499ohms
R137 499ohms
Low Noise,Rail-to-Rail,Diff ADC Drivr
U17 AD8139ARZ
R136 100ohms
R146 100ohms
R138 499ohms
R147 499ohms
LOCAL_5V_ADC
C12 0.001uF
C13 0.001uF
C51 0.1uF
C49 0.1uF
C58 0.1uF
C15 0.1uF
GNDA
R145 0ohms
0.1uF C54
VIO
GND
R21 100ohms
R36 100ohms
3V LVDS High Speed Diff Driver
U91 DS90LV011ATMF
3V LVDS CMOS Diff Receiver
U37 DS90LT012ATMF
U36 DS90LT012ATMF
U92 DS90LV011ATMF
ADC_CLK
ADC_DCO
ADC_DAT
ADC_CNV
16-Bit, 6MSPS PulSAR Differential ADC
A07625BCPZ
U19
Fair-Rite 2512067007Y3
L13
LOCAL_2.5V_ADC
R37 10Kohms
R38 10Kohms
C16 0.1uF
C56 0.1uF
C61 0.1uF
BP14 0.01uF
C52 10uF
C57 10uF
C68 10uF
See Figure 31 of the AD7625 datasheet for PCB layout reccomendations.
+12V
12V Ultra-Low-Iq Reg w/POR-5.0V
U24 MAX8881EUT50+T
ENA_ADC_5V
R42 2Kohms
C63 2.2uF
C64 2.2uF
+3.3V
BP17 0.1uF
BP30 0.1uF
BP16 0.1uF
BP21 0.1uF
+5.4V
25V LDO Voltage Reg
U25 TPS79325DBVR
ENA_ADC_2.5V
R43 2Kohms
R156 0ohms
C62 2.2uF
C10 2.2uF
BP51 0.01uF
R24 2Kohms
C17 2.2uF
BP44 0.01uF
C53 2.2uF
VIO

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EED Department	DESIGNATOR	Craig Drennan	DATE 02.2015
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Z:\UBS\Phase0of2 MPM ACCEL\PCB Design -- ACCEL\phase0of2_ACCEL_Physics.dsn

BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

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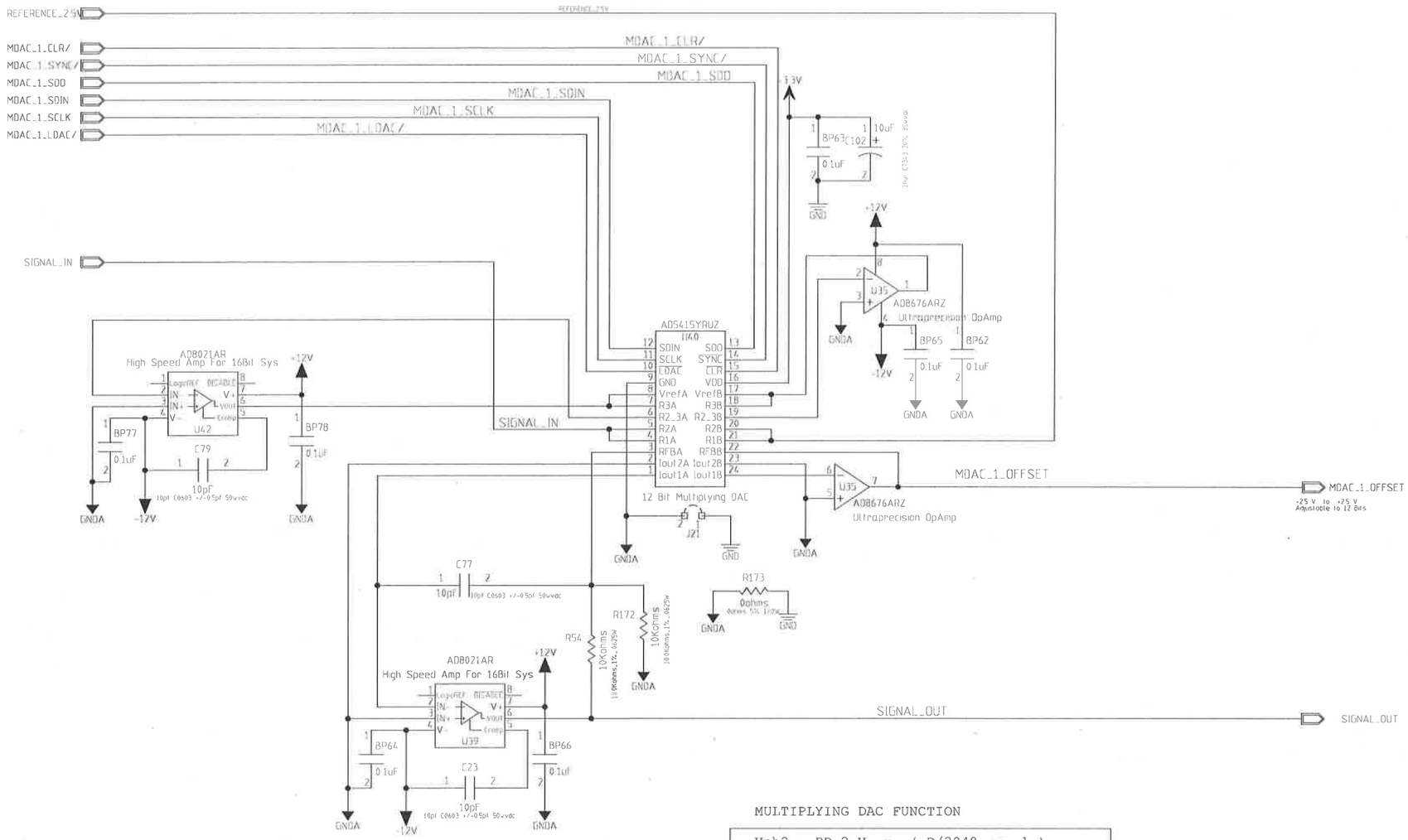
B	0000-EB-282413	

Schematic Page 01 of 01

Multiplying DAC, page 7 of 16



MULTIPLYING DAC FUNCTION

Vph2 = PD_2_V x (D/2048 - 1)

Digital Input	Analog Output (Vph1)
1111 1111 1111	+PD_2_V
1000 0000 0000	0
0000 0000 0001	PD_2_V (1/2048 - 1)
0000 0000 0000	-PD_2_V

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EED Department	ORIGINATOR	Craig Drennan	DATE 02 2015
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Z:\RDBS\Phase3\BPL ACCEL-PLB Users --- ACCEL Schmidt3_ACCEL.150605.sch Filter DAC Multiplyphase3_ACCEL.pdf

BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

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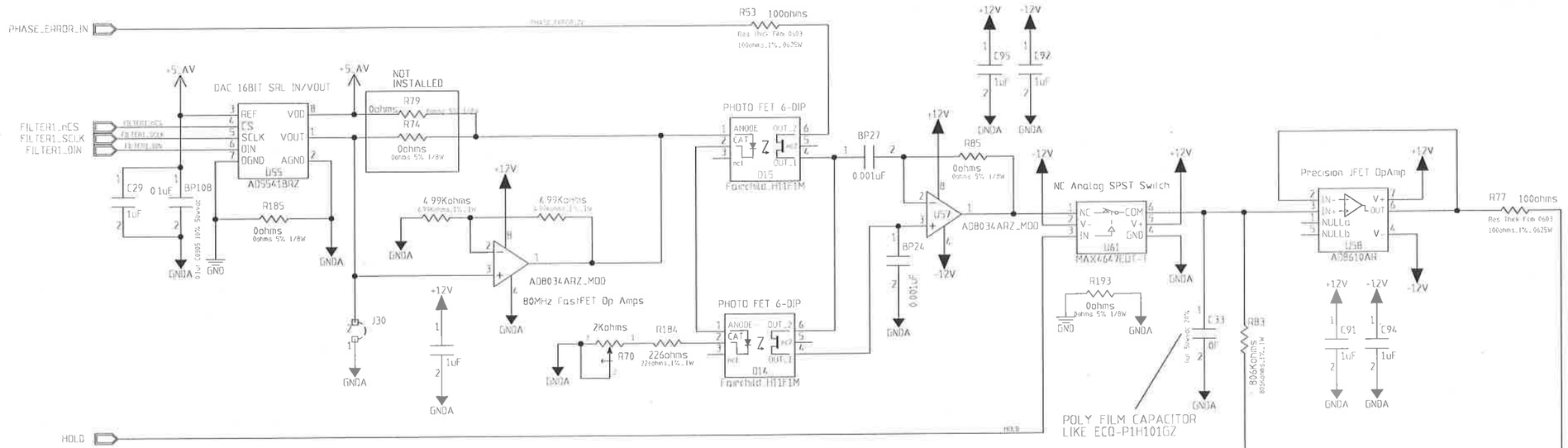
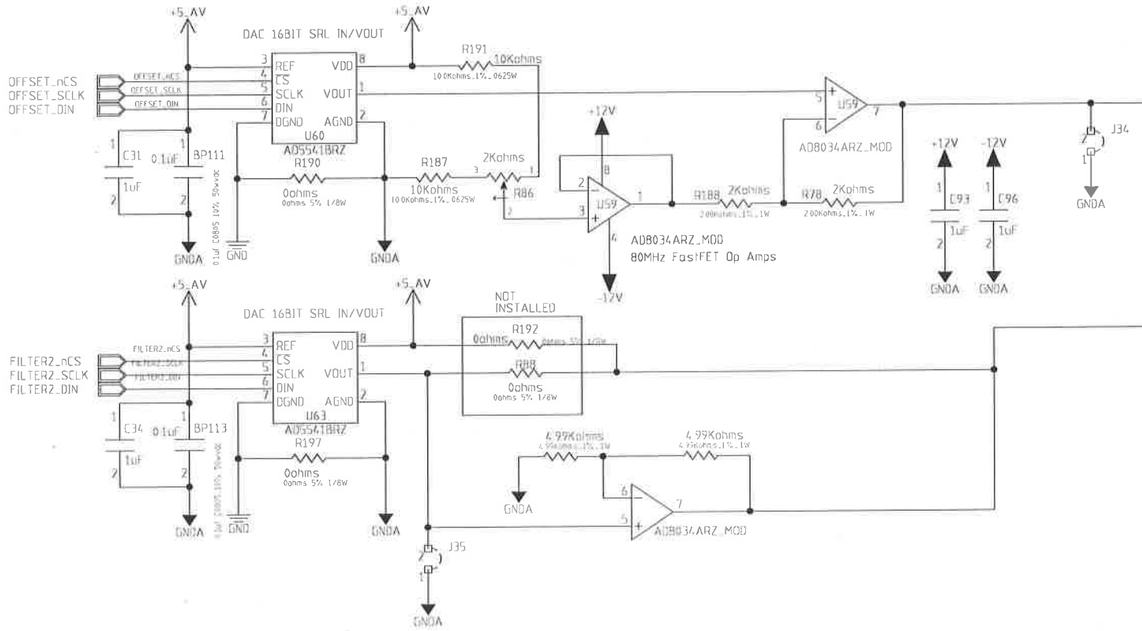
Sheet 7 of 16

Filter and Hold, page 8 of 16





MODIFIED 8/5/2015 11:27 PM			
FED Department	ORIGINATOR	Craig Drennan	DATE 02/2015
	DRAWN	Craig Drennan	DATE 02/2015
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BOOSTER ACCELERATOR
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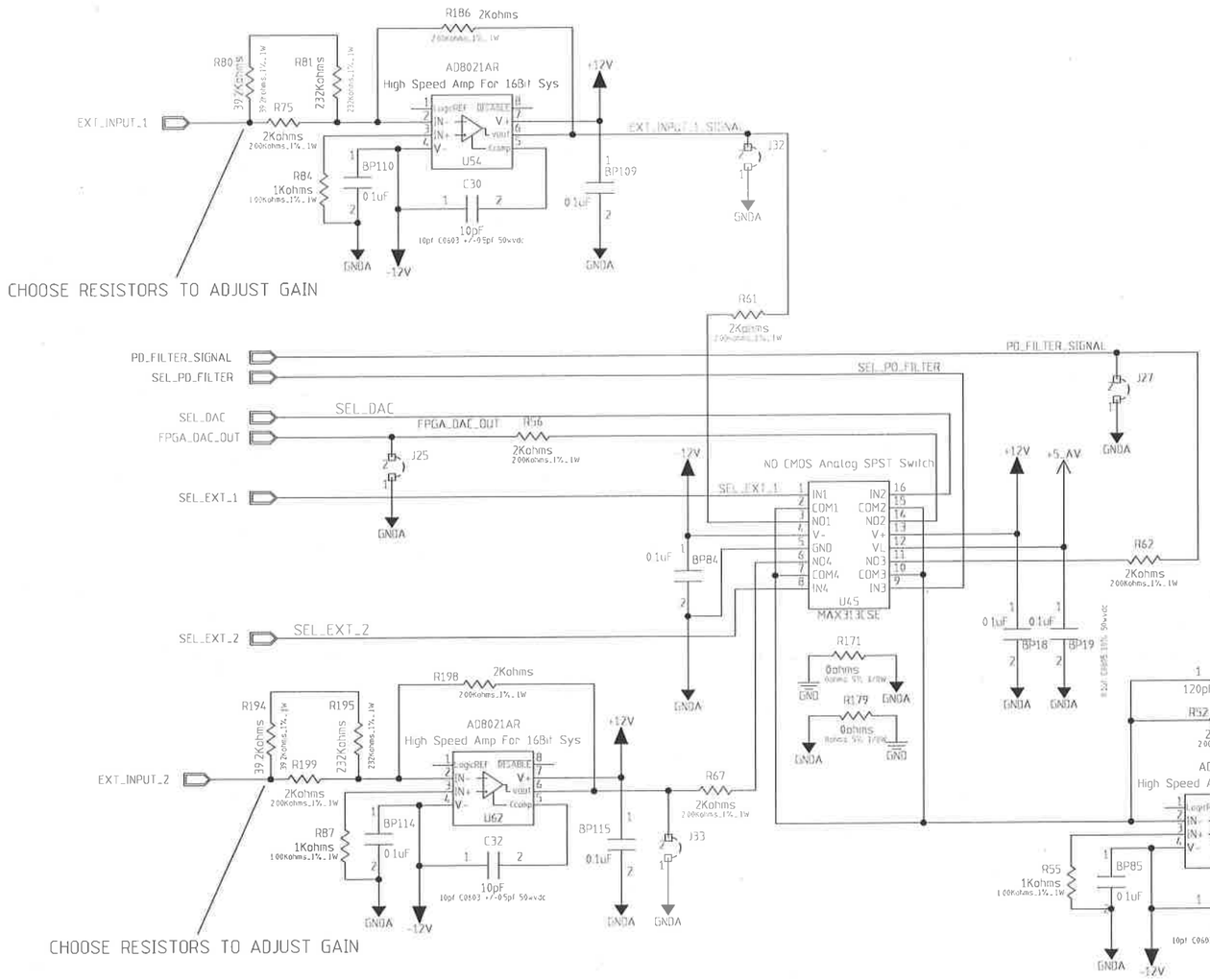
Output Sum Mux, page 9 of 16



MODFIED 6/18/2015 2:46:12 PM			
EED Department	ORIGINATOR	Craig Drennan	DATE 02 2015
	DRAWN	Craig Drennan	DATE 02 2015
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Z:\MCS\Phase0e13\MPL ACCEL\PCB Design -- ACCEL\phase0e12_Accel_15Feb15.dwg

BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

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B	0000-EB-282413	

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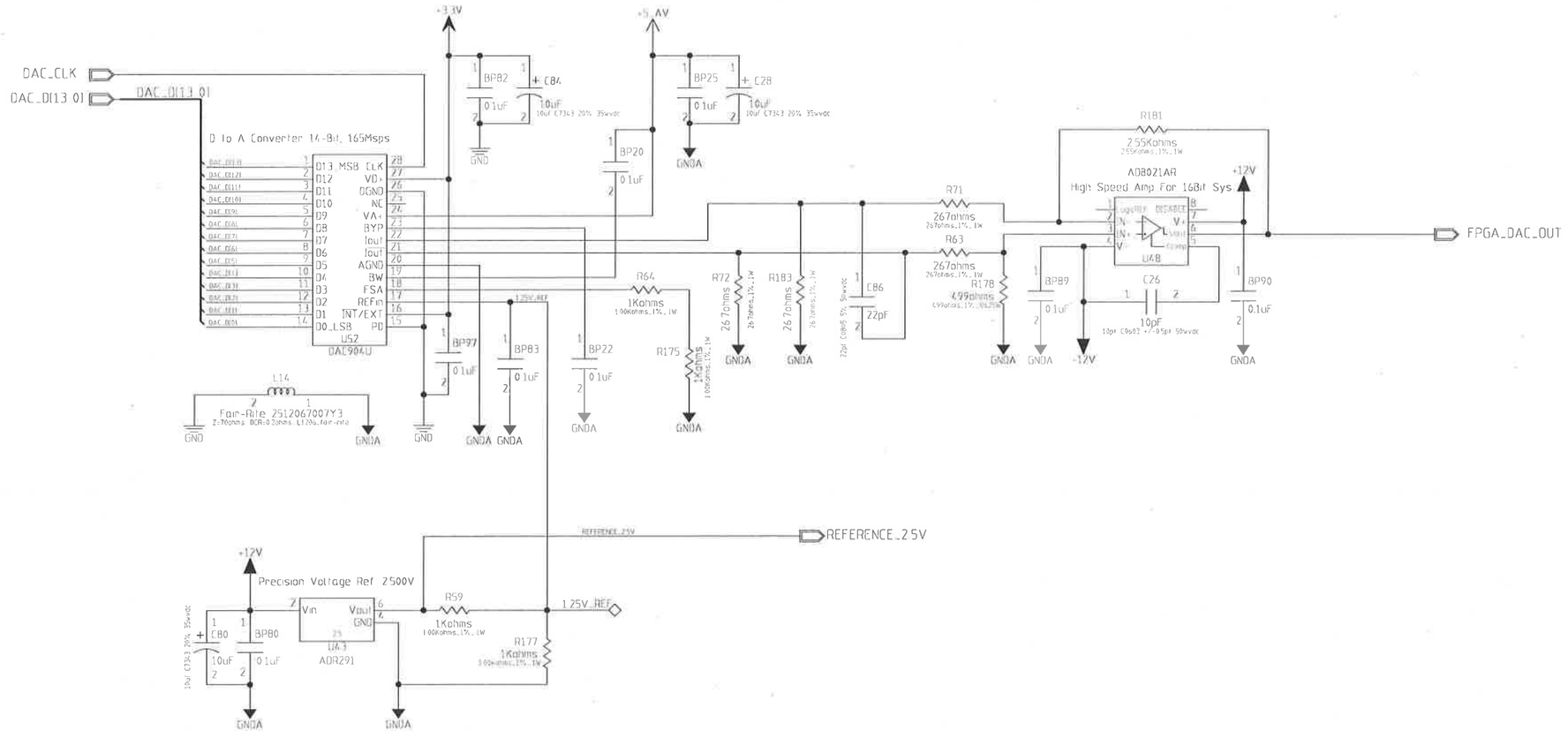

MODFIED 6/18/2015 2:47:16 PM			
FEO Department	ORIGINATOR	Craig Drennan	DATE 4/2/2015
	DRAWN	Craig Drennan	DATE 4/2/2015
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Z:\MDSVMnosequels\MPL ACCEMPLE Design - Accelerendsequels\Accel_Sys\Accel.dwg

BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

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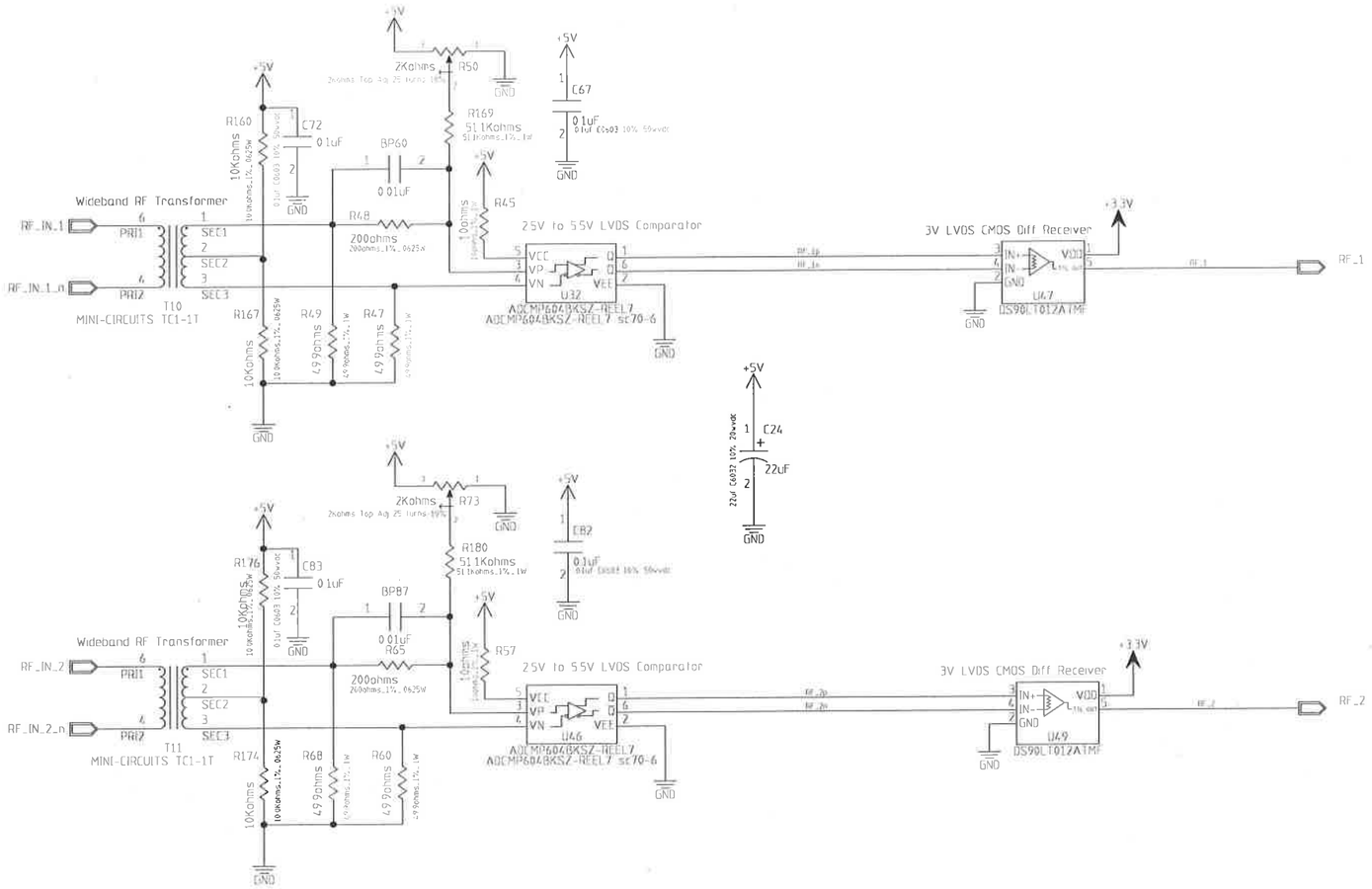
RF Inputs, page 11 of 16



MODIFIED 6/18/2015 2:48:05 PM			
FEO Department	ORIGINATOR	Craig Drennan	DATE 02.2015
	DRAWN	Craig Drennan	DATE 02.2015
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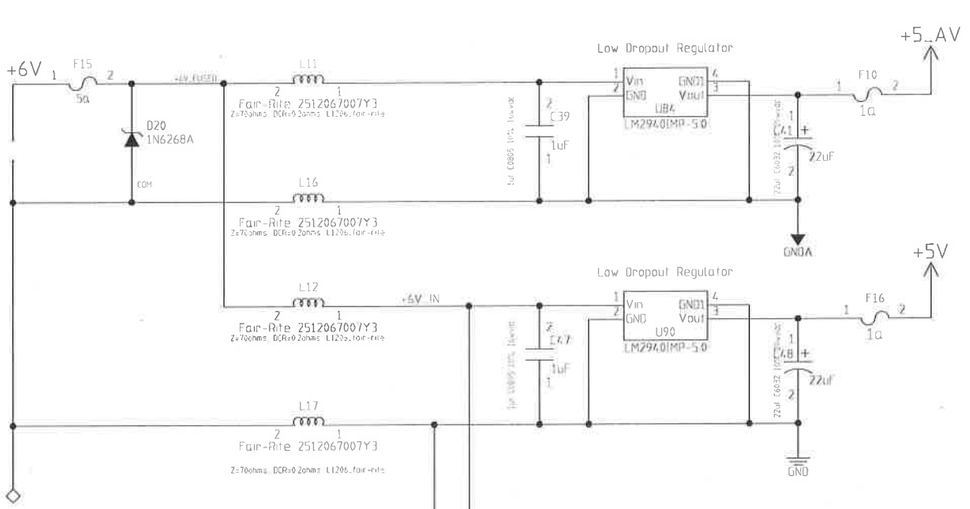
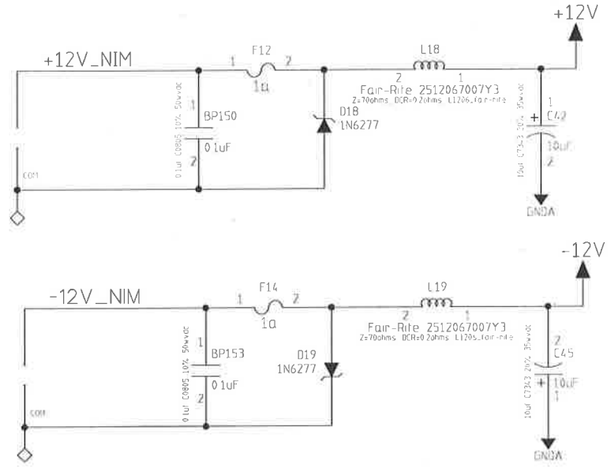
Z:\IOBS\Phase0e13 FNPL ACCEL\PCB Design -- ACCEL\phase0e13_ACCEL_15V505_with Filter BAC Mod\phase0e13_ACCEL.pri

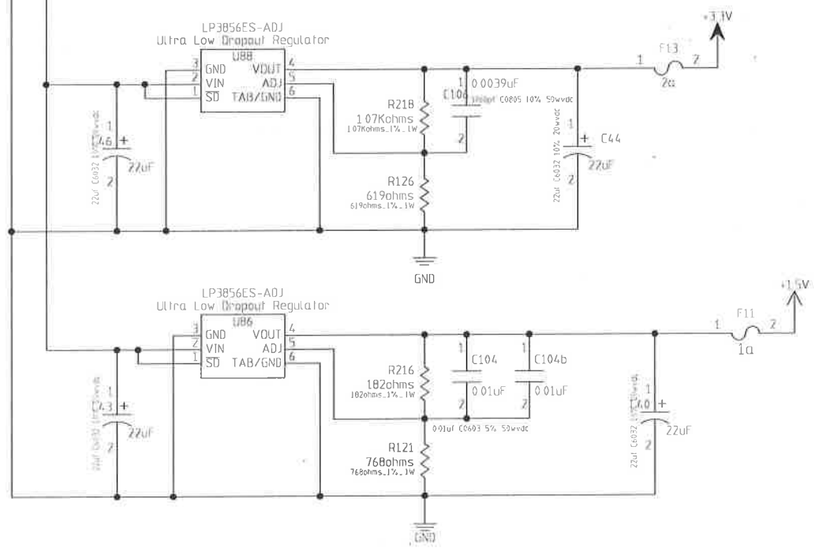
BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

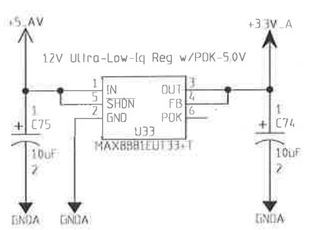
SIZE	DRAWING NUMBER	REV
B	0000-EB-282413 Schematic Page 01 of ##	

Power Regulators, page 12 of 16









MODFIED 6/18/2015 2:57:02 PM			
EED Department	DESIGNATOR	Craig Drennon	DATE 02/2015
	DRAWN	Craig Drennon	DATE 02/2015
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Z:\IOS\APhase\Be13 MPL ACCELXPCB Design — ACCEL\phase\be13_ACCEL_1519605.SchDoc Filter: DAC Multi-phase\be13_ACCEL.prj

BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	Schematic Page 01	REV
B	0000-EB-282413	OF 01	

FPGA Memory, page 13 of 16

U53

Altera Cyclone EP1C6 Device

EP1C6Q240C8

ECO New P/N AT45DB021E-SSHN

BOOSTER ACCELERATOR

PHASE-LOCK CONTROLLER

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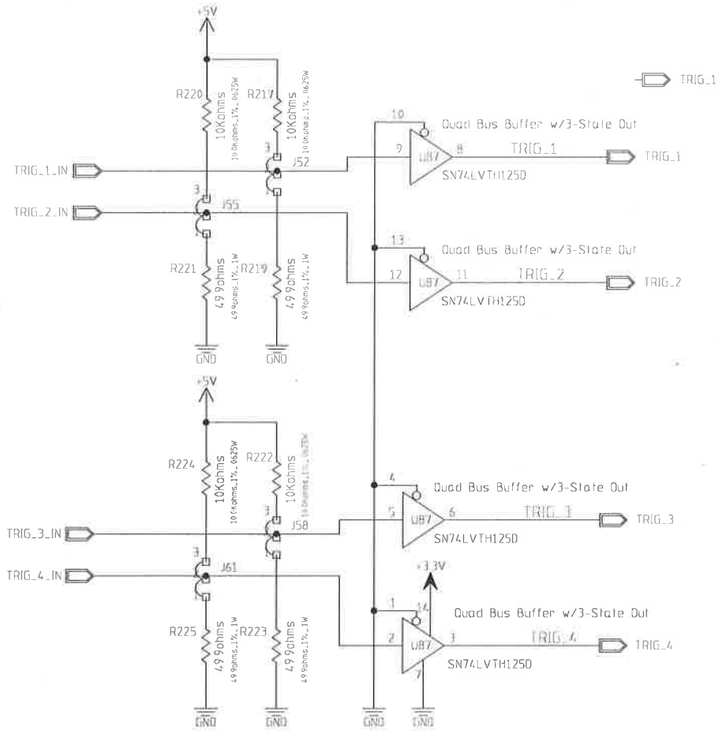
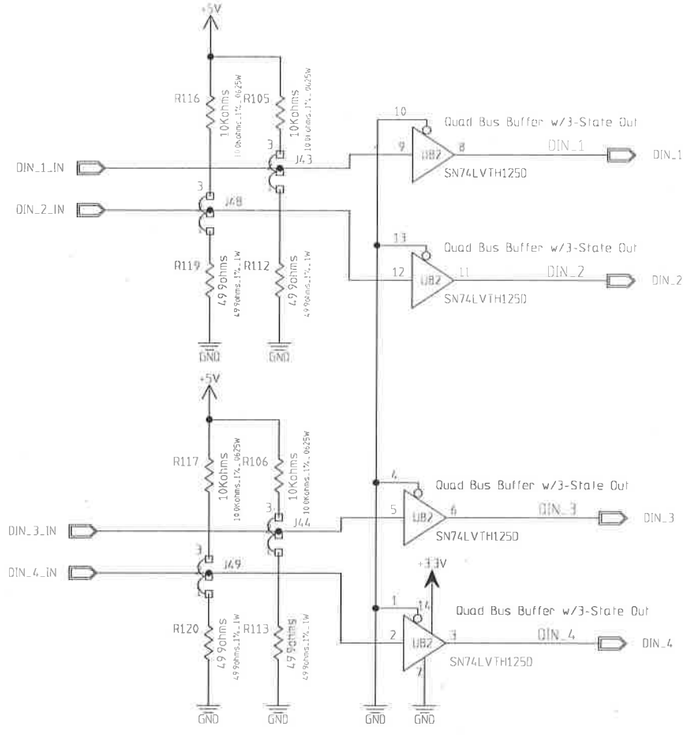
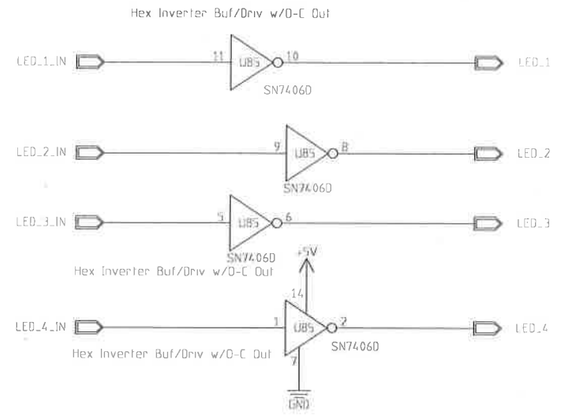
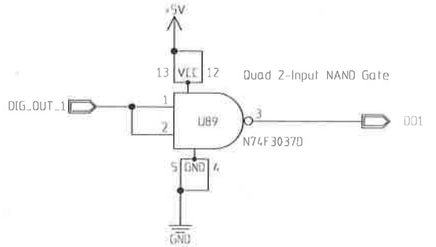
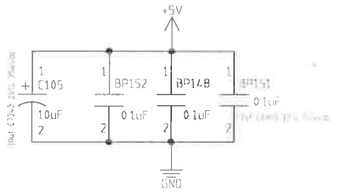
Digital IO, page 14 of 16

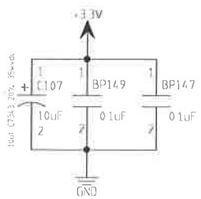












MODIFIED 6/18/2015 2:59:43 PM			
EED Department	ORIGINATOR	Craig Drennan	DATE 02/2015
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	CHECKED	Craig Drennan	DATE 02/2015
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BOOSTER ACCELERATOR
PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	Sheet no Page 01 of 01	REV
B	0000-EB-282413		

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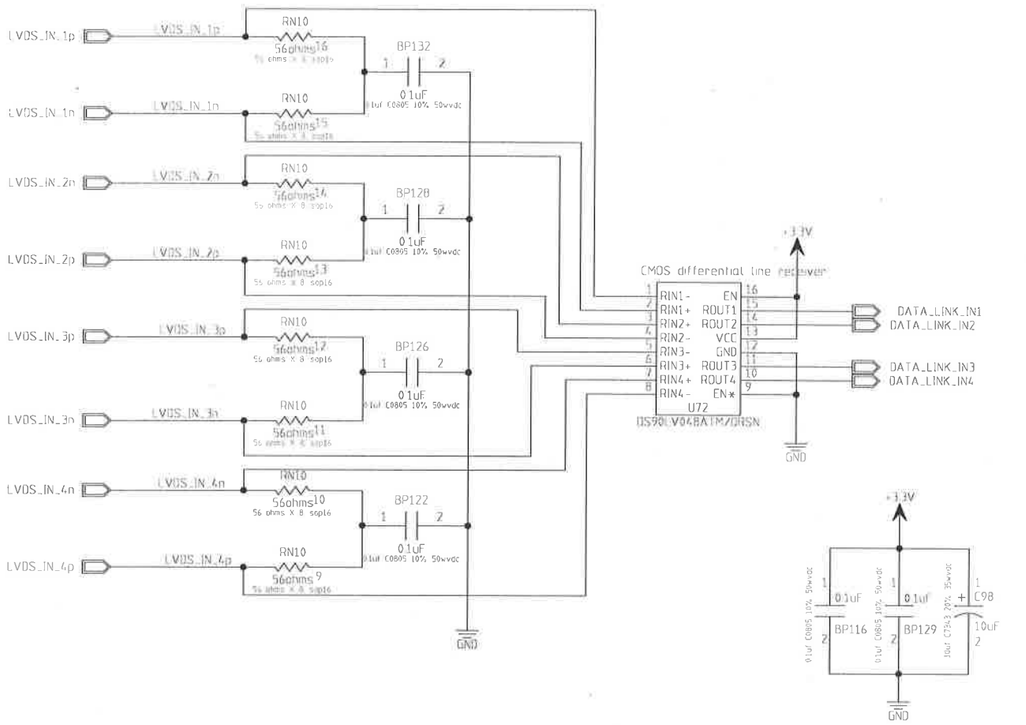

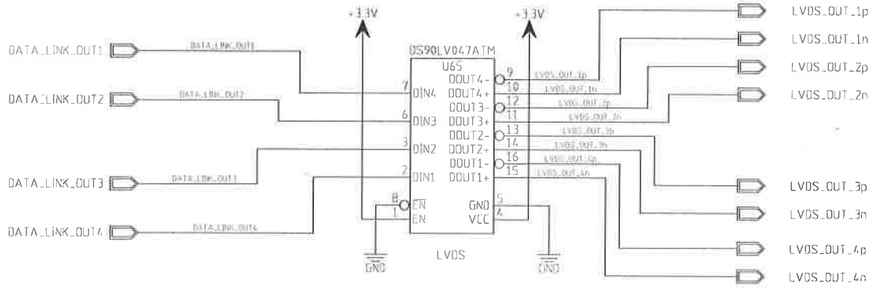

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EED Department

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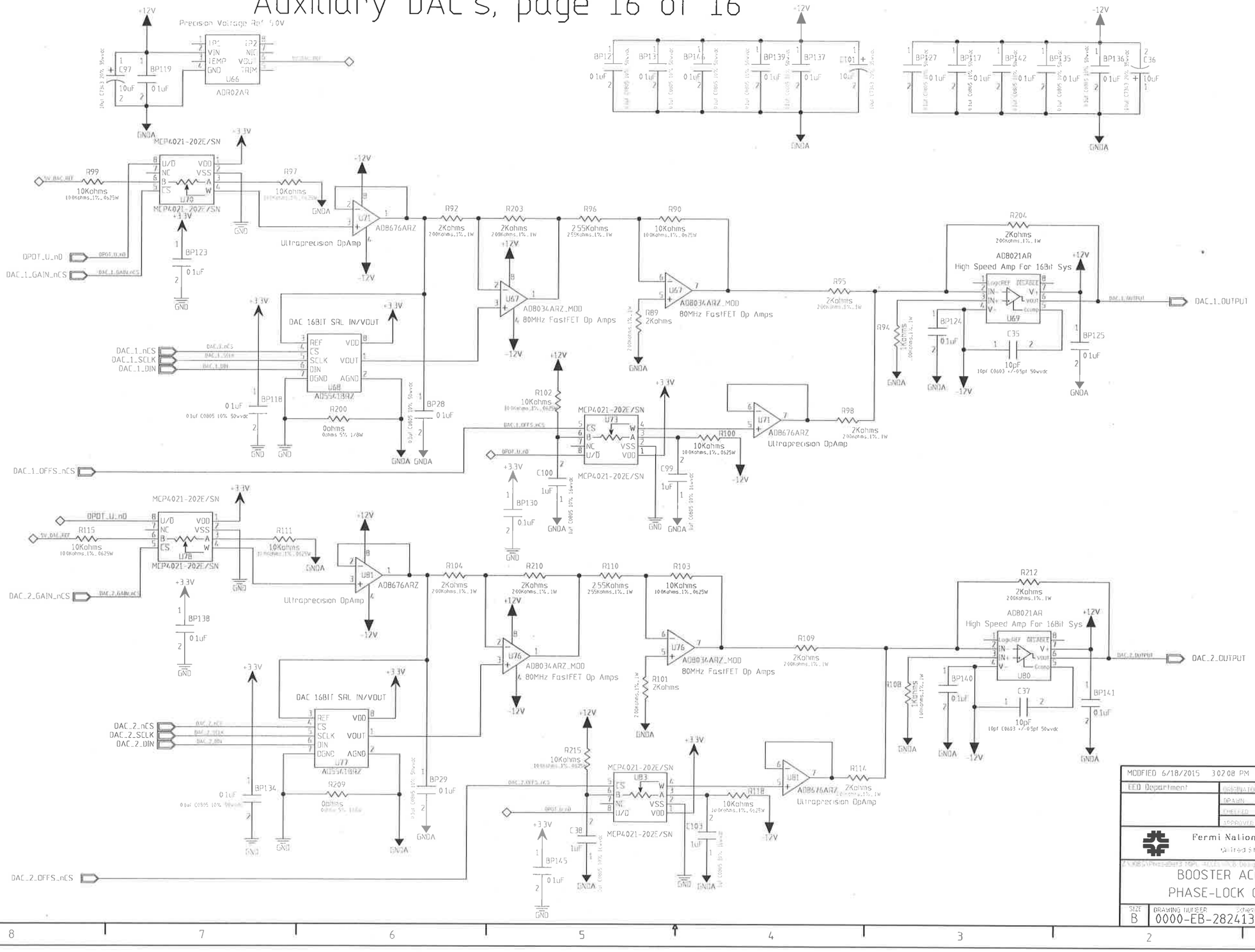
Schematic Page 15 of 16

Auxiliary DAC's, page 16 of 16