

# Specification for the Sequenced Chassis Control Card

Craig Drennan

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## I. Introduction

The Sequenced Chassis Control Card (dwg# 498222) is a revision of the Multiple Power Supply Interface Chassis, Chassis Control Card (dwg# 498139) used initially for controlling the capacitor charging supplies in the LINAC Marx Modulator. The charging system has 4 sets of 4 supplies and 1 set of 3 supplies. Where the initial Control Card turned all 5 sets of charging supplies on at once, the Sequenced Chassis Control Card will be able to turn on each of the 5 sets in an adjustable sequence.

The majority of the signals in and out of the card go through a 3x32 pin VME style connector at the rear of the module. This connector brings in signals, through a custom backplane, from other circuit cards installed in the rear of the chassis and the Control Card outputs signals across the backplane to other rear mounted cards and other front mounted cards installed in the front of the chassis. Figure I.1 is a photo of the Control Chassis installation for the first LINAC Marx Modulator.

Figure I.2 is a photo of the rear of the PS Control Chassis. These cards in the rear interface the control cards in the front to the power supplies and the equipment outside the chassis.

Figure I.3 is a photo of the original Chassis Control Card, and Figure I.4 is a photo of the PS Control Interface Cards.

In order to implement the adjustable charging supply sequence, a programmable logic device (CPLD) will be added to the existing components of the Chassis Control Card. The device currently selected is the Altera Max V CPLD device, part number 5M570ZT100C5N. This device provides 570 Logic Elements (LE) and 74 user IO pins in a TQFP leaded package. Additional supporting components such as 3.3V and 1.8V voltage regulators, a clock oscillator, and backplane signal input buffers that are 3.3V logic devices with 5V inputs will be added to the current Chassis Control Card. Nearly all of the pre-existing circuitry on the Chassis Control Card will be replicated on the new card.

Additionally, the IO connections to the backplane will be identical, with the addition of the 5 charging supply sequence pulses. Table I.1 lists the pin out for the backplane connector.

This document and other supporting documents are available on the DocDB database at Beams-doc-5322-v1.

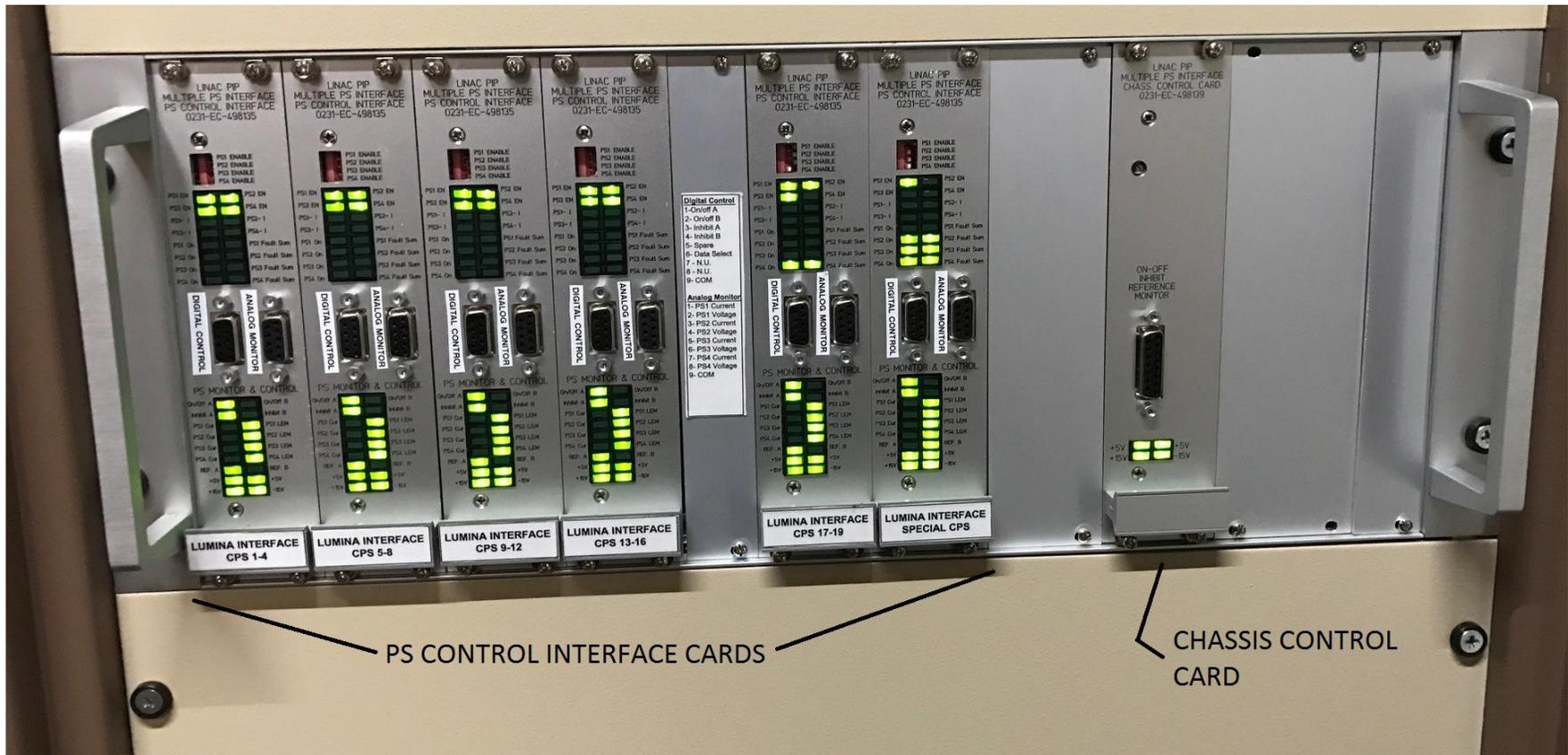


Figure I.1 Existing PS Control Chassis for the LINAC Marx Modulator.

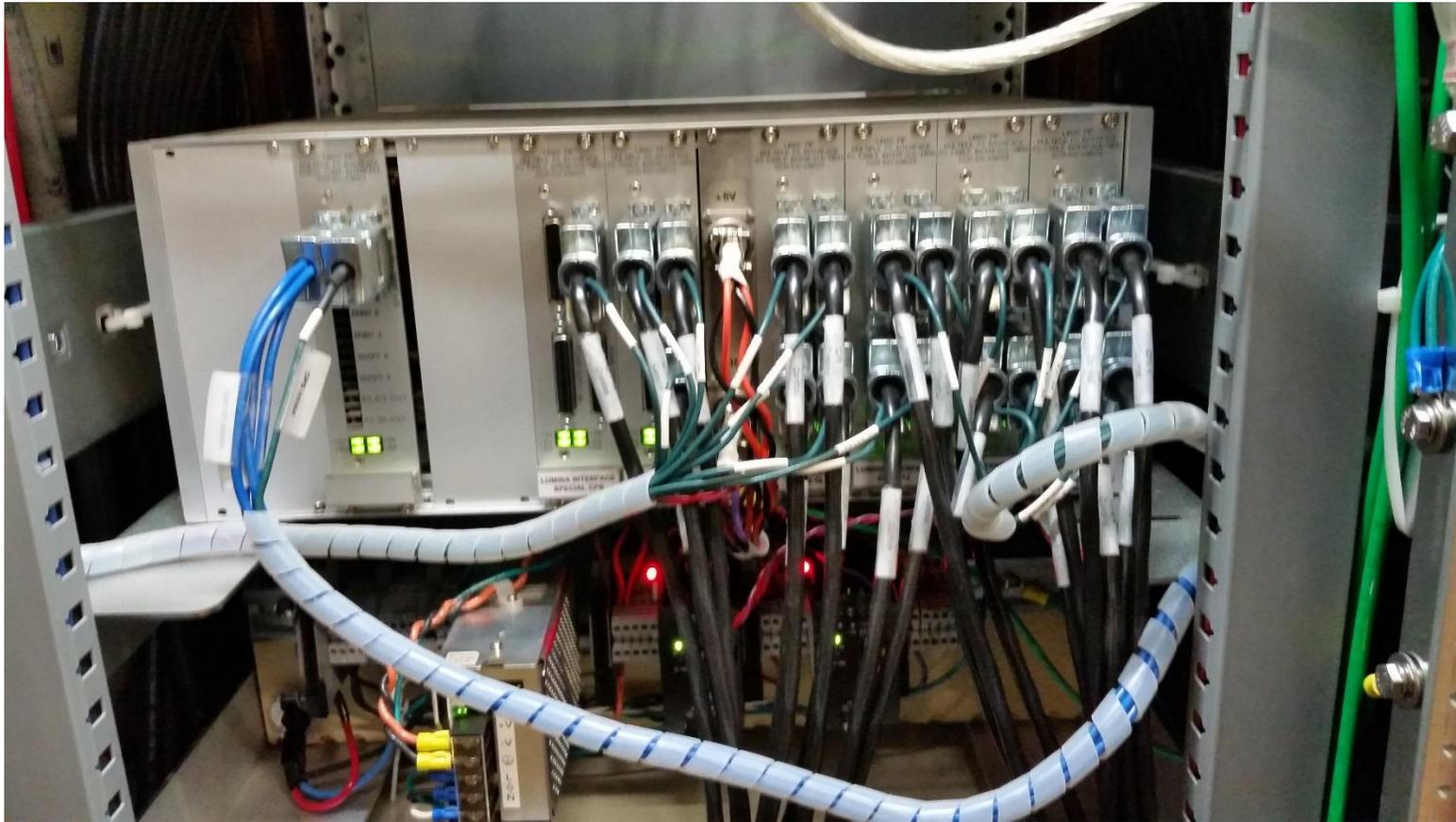


Figure I.2 PS Control Chassis Rear.



Figure I.3 The initial version of the Chassis Control Card.

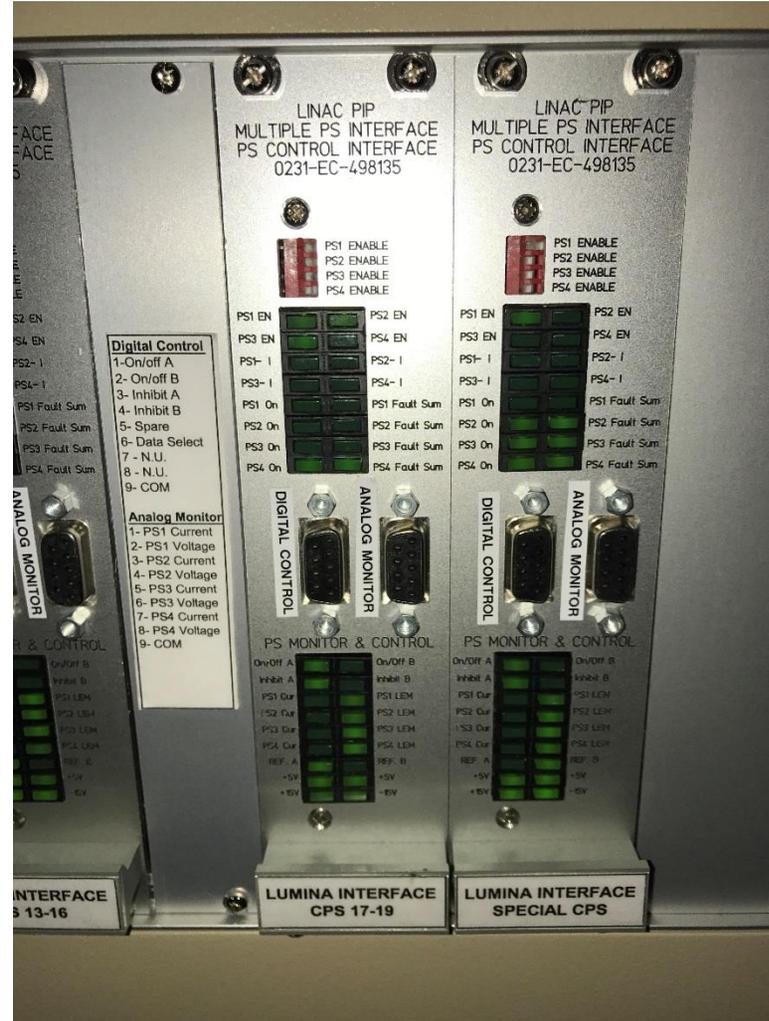


Figure I.4 The PS Control Interface Card.

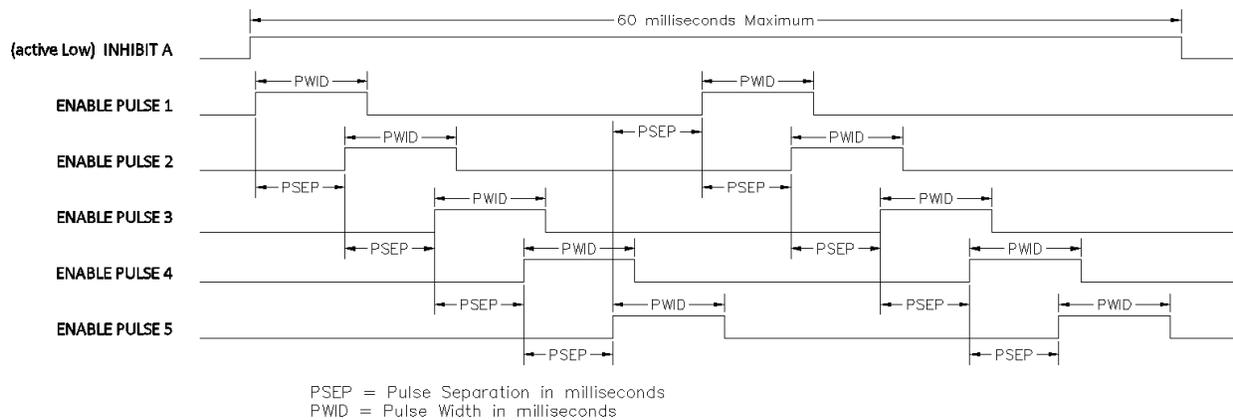
Table I.1 Pin out for the backplane connection.

	A	B	C
1	5V Common	5V Common	5V Common
2	5V Common	5V Common	5V Common
3	+5 V Supply	+5 V Supply	+5 V Supply
4	+5 V Supply	+5 V Supply	+5 V Supply
5	On/Off A TTL -- IN	On/Off B (Isolated) IN +	On/Off A (Isolated) IN +
6	On/Off B TTL -- IN	On/Off B (Isolated) IN –	On/Off A (Isolated) IN –
7	Inhibit A TTL -- IN	Inhibit B (Isolated) IN +	Inhibit A (Isolated) IN +
8	Inhibit B TTL -- IN	Inhibit B (Isolated) IN –	Inhibit A (Isolated) IN –
9			Analog VCAP IN (+)
10			Analog VCAP IN (-)
11			
12		Buffered Ref A to Backplane	Buffered Ref B to Backplane
13	On/Off A to Backplane	On/Off B to Backplane	
14	Inhibit A to Backplane	Inhibit B to Backplane	
15			
16			
17			Sequence Pulse 3 (J78)
18	Sequence Pulse 5 (J76)	Sequence Pulse 1 (J80)	Sequence Pulse 4 (J77)
19	P.S. On Status -- IN	Sequence Pulse 2 (J79)	P.S. On Status (Dry Contact) +
20	P.S. Fault Status -- IN		P.S. On Status (Dry Contact) –
21			P.S. Fault Status (Dry Contact) +
22			P.S. Fault Status (Dry Contact) –
23			P.S. On Status (Buffered)-- OUT
24			P.S. On Status (Fiber)-- OUT
25	Analog Ref A (–)	Analog Ref A (+)	P.S. Fault Status (Buffered)-- OUT
26	Analog Ref B (–)	Analog Ref B (+)	P.S. Fault Status (Fiber)-- OUT
27	+15 V Supply	+15 V Supply	+15 V Supply
28	+15 V Supply	+15 V Supply	+15 V Supply
29	-15 V Supply	-15 V Supply	-15 V Supply
30	-15 V Supply	-15 V Supply	-15 V Supply
31	15 V Common	15 V Common	15 V Common
32	15 V Common	15 V Common	15 V Common

## II. Capacitor Charging Control Sequence

The numbered items below specify the capacitor charging control sequence.

1. The maximum charging interval in which each of the charging supplies needs to provide their contributions to the Marx Modulator capacitors is 60 milliseconds (ms).
2. The sets of charging supplies are controlled by signals that enable the supplies when High and inhibit the supplies when Low.
3. The signal "Inhibit A TTL In" controls the running of the sequence. When this signal goes from Low to High the sequence of charging supply enable pulses begins.
4. If the Inhibit A signal goes Low before the sequence is complete, the sequence is terminated and all of the charging supplies are inhibited.
5. If the VCAP analog input voltage reaches the Reference A voltage level a comparator circuit signals the logic and the sequence is terminated and all of the charging supplies are inhibited.
6. Two settable parameters define the sequence of charging supply enable pulses. Each of these parameters have units of milliseconds. One millisecond is the smallest increment for the Pulse Width parameter. One half millisecond is the smallest increment for the Separation parameter.
  - a. Pulse Separation: This is the time in milliseconds between the start of one enable pulse and the next.
  - b. Pulse Width: This is the duration of each of the enable pulses.
7. The sequence of five enable pulses will repeat until the sequence is terminated by the occurrence of the VCAP inhibit or Inhibit A going low.



8. The Pulse Width parameter is to be adjustable from 1 ms to 16 ms. This will be done with a 16 position (4 bit) hexadecimal encoded rotary switch on the front panel. The increment resolution will be 1 ms.
9. The Separation parameter is to be adjustable from 1 ms to 7 ms. This will be done with a 16 position (4 bit) hexadecimal encoded rotary switch on the front panel. The increment resolution will be 0.5 ms.

### III. Preliminary Design

The card has an analog section and a digital section. The analog section is simple. It buffers the Reference A and Reference B signals onto the Power Supply Interface Chassis backplane and out onto the front panel DSUB connector. The VCAP Reference A comparator is also in the analog section.

The digital section constitutes the majority of the card. With the exception of the PS Fault Status Fiber and PS On Status Fiber outputs to the backplane, all digital inputs and outputs go through the CPLD. This adds flexibility to the cards logic and provides for more control at power on and resets. The following tables list the digital inputs and outputs. A preliminary schematic is available on the DocDB database at Beams-doc-5322.

Table III.1 Digital inputs to the card.

	Connection	Name	Description
1	A19	PS ON STATUS	Power supply on/off status signal.
2	A20	PS FAULT STATUS	Power supply fault summation status signal.
3	A7	INHIBIT A TTL IN	Power supply inhibit/enable signal, system A.
4	C7, C8	INHIBIT A ISO IN	Power supply inhibit/enable signal, system A, optically isolated input.
5	A8	INHIBIT B TTL IN	Power supply inhibit/enable signal, system B.
6	B7, B8	INHIBIT B ISO IN	Power supply inhibit/enable signal, system B, optically isolated input.
7	A5	ON/OFF A TTL IN	Power supply On/Off control signal, system A.
8	C5, C6	ON/OFF A ISO IN	Power supply On/Off control signal, system A, optically isolated input
9	A6	ON/OFF B TTL IN	Power supply On/Off control signal, system B.
10	B5, B6	ON/OFF B ISO IN	Power supply On/Off control signal, system B, optically isolated input
11		VCAP vs. REF A	Analog comparator bit that determines the end of the sequence.
12	J32	SPARE 1	A spare buffered input to the CPLD

Table III.2 Digital output to the chassis backplane.

	Connection	Name	Description
1	C23	PS ON STATUS OUT	Power supply on/off status signal out to the backplane.
2	C19, C20	PS ON STATUS CONTACTS	Power supply on/off status signal out form C relay contact. 2 A @ 30 VDC, 1 A @ 120 VAC
3	C25	PS FAULT STATUS OUT	Power supply fault status signal out to the backplane.
4	C21, C22	PS FAULT STATUS CONTACTS	Power supply fault status signal out form C relay contact. 2 A @ 30 VDC, 1 A @ 120 VAC
5	A14	INHIBIT A to BACKPLANE	Power supply inhibit/enable signal, system A, out to backplane.
6	B14	INHIBIT B to BACKPLANE	Power supply inhibit/enable signal, system B, out to backplane.
7	A13	ON/OFF A to BACKPLANE	Power supply On/Off control signal, system A out to backplane.
8	B13	ON/OFF B to BACKPLANE	Power supply On/Off control signal, system B out to backplane.
9	B18	SEQUENCE PULSE 1	Group 1 charging supply sequenced enable pulse, system A.
10	B19	SEQUENCE PULSE 2	Group 2 charging supply sequenced enable pulse, system A.
11	C17	SEQUENCE PULSE 3	Group 3 charging supply sequenced enable pulse, system A.
12	C18	SEQUENCE PULSE 4	Group 4 charging supply sequenced enable pulse, system A.
13	A18	SEQUENCE PULSE 5	Group 5 charging supply sequenced enable pulse, system A.

Table III.3 Digital signals out to the front panel DSUB connector.

	Connection	Name	Description
1	DSUB-1	ON/OFF A	Power supply on/off status signal, system A, out to the front panel.
2	DSUB-2	VCAP COMPARE	Results of the VCAP vs. Reference A Comparison.
3	DSUB-3	INHIBIT A	Power supply inhibit/enable signal, system A, out to the front panel.
4	DSUB-4	ENABLE PULSE 5	Group 5 charging supply sequenced enable pulse, system A
5	DSUB-5	REF A	Analog power supply reference monitor, system A.
6	DSUB-6	ENABLE PULSE 3	Group 3 charging supply sequenced enable pulse, system A
7	DSUB-7	PS ON STATUS	Power supply on/off status signal out to the front panel.
8	DSUB-8	ENABLE PULSE 1	Group 1 charging supply sequenced enable pulse, system A
9	DSUB-9	ON/OFF B	Power supply on/off status signal, system B, out to the front panel.
10	DSUB-10	ground	Ground reference.
11	DSUB-11	INHIBIT B	Power supply inhibit/enable signal, system B, out to the front panel.
12	DSUB-12	ENABLE PULSE 4	Group 4 charging supply sequenced enable pulse, system A
13	DSUB-13	REF B	Analog power supply reference monitor, system B.
14	DSUB-14	ENABLE PULSE 2	Group 2 charging supply sequenced enable pulse, system A
15	DSUB-15	PS FAULT STATUS	Power supply fault status signal out to the front panel.

Note: Signal driven out to the DSUB-15 connector will have series 3k Ohm current limiting resistors.

Table III.4 Front panel LED outputs from the CPLD

	Connection	Name
1	LED-1	INHIBIT A
2	LED-2	INHIBIT B
3	LED-3	PS ON STATUS
4	LED-4	PS FAULT STATUS

Table III.5 Other CPLD IO.

	<b>Name</b>	<b>Description</b>
4 inputs	Enable Pulse Width	4 Bit value set by a hexadecimal encoder switch that set the charging supply enable pulse widths in milliseconds.
4 inputs	Enable Pulse Separation	4 Bit value set by a hexadecimal encoder switch that set the charging supply enable pulse separation in increments of 0.5 milliseconds.
16 IO	Test Expansion Headers	2 each, 8x2 pin, 0.100 pitch headers for logic testing and expansion.
	JTAG Connector	CPLD JTAG connection for programming the chip.
1 input	RESET IN	External power up reset pulse
1 input	CLOCK 50MHz	Logic clock input from a 50 MHz clock oscillator