## BPM Requirements

The BPM signals pass through an input attenuator (-7 dB), then a diplexer filter (LPF fc=30 MHz and a BPF fc= 201MHz) followed by a mixer which down-converts the signal to 28.3 MHz. The output of the mixer has a LPF fc=30MHz and then a gain stage using a CCA821. These conditioned signals are fed to a 12-channel digitizer. Timing for the digitizer and the CPU is performed by the Booster Timing Module. Digitizer timing consists of a Sync and an Arm (or gate) which arms the measurement and then the sync provides the turnmarker every 84 buckets. Input to the timing generator are

1. The Booster RF Clock (BRF) operates from 38 MHz to 52.808 MHz,

2. Booster LO operating from 66 MHz to 81.1 MHz,

3. Booster CHOP ON Delayed

4. TCLK operating at 10MHz and asynchronous to the beam containing accelerator complex-wide commands

5. 100 MHz fixed frequency clock.

6. 120 MHz fixed frequency clock.

7. 16.0 MHz VME clock.

The operation of the DDC module is controlled by two inputs that are common for all eight channels. They are the SYNC and ARM signals. The digitizing clock is 250 MHz internal to the DDC module. The DDC oversamples the 23.0 MHz producing ~10 samples per cycle. The 201.25 Mhz signal is undersampled by the DDC 250 MHZ sampling rate, producing a 48.75 MHz signal which is them down-converted to baseband by the numerical NCO in the DDC.

The crate is controlled by a commercial CPU and timed synchronously to the Booster beam by the TGF-II. The output of the transition channel is a constant 23.0 MHz frequency as a result of 38 to 52.8 MHz mixed with the LO signal sweeping from 66MHz to 81.1 MHz.

## Number of BPM’s to be Instrumented

There are **51 BPM detectors**, providing **102 position measurements** that need to be instrumented. Appendix A lists the measured BPM positions according to the location in the Booster gallery where the electronics is expected to reside. Appendix B shows pre-upgrade rack layouts for the BPM electronics to indicate the space available for the new electronics.

**BPM Locations**

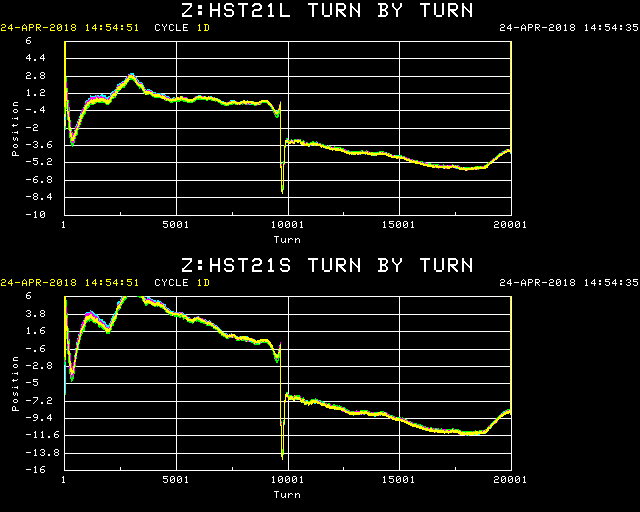
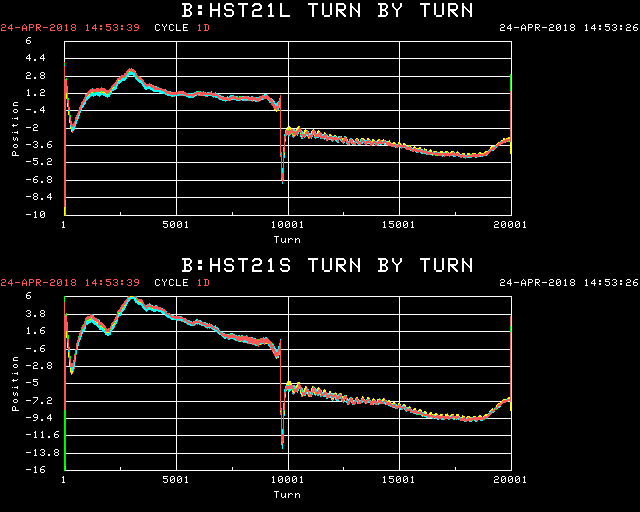
The 8-channel Transition cards are installed side-by-side with the12 channel digitizers (DDC) in a VXS crate. The number varies depending on the Booster period. The table below contains the number of BPMs and the rack of installation.

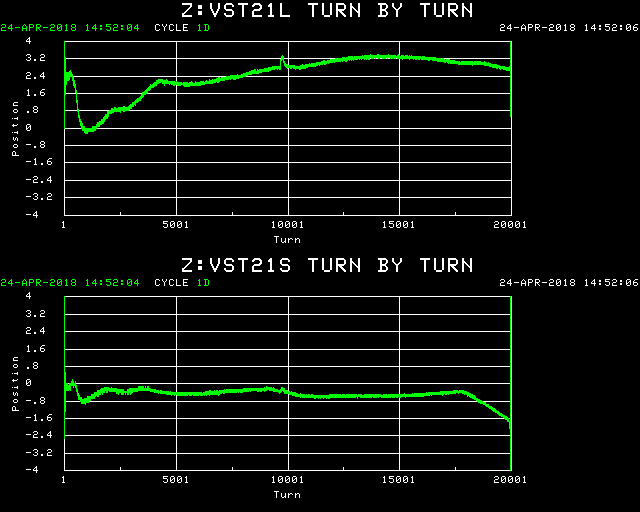
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Rack Number** | **Period** | **Number of BPMs** | **Number of Pickups** | **No Timing Board** | **No Transition 8 ChannelBrds** |
| G20-RR1 | 18-20 | 6 | 12 Hor 12 Vert | 1 | 3 |
| G01-RR5-2 | 21-23 | 6 | 12 Hor, 12 Vert | 1 | 3 |
| G01-RR6-1 | 24-02 | 13 | 26 Hor, 26 Vert | 1 | 7 |
| G01-RR6-2 | 09-11 |  |  |  |  |
| G01-RR6-3 |  |  |  |  |  |
| G11-RR6-1 | 06-08 | 14 | 28 Hor, 28 Vert | 1 | 7 |
| G11-RR6-2 | 03-05 |  |  |  |  |
| G11-RR6-3 |  |  |  |  |  |
| G14-RR1 | 12-14 | 6 | 12 Hor, 12 Vert | 1 | 3 |
| G17-RR2 | 15-17 | 6 | 12 Hor, 12 Vert | 1 | 3 |

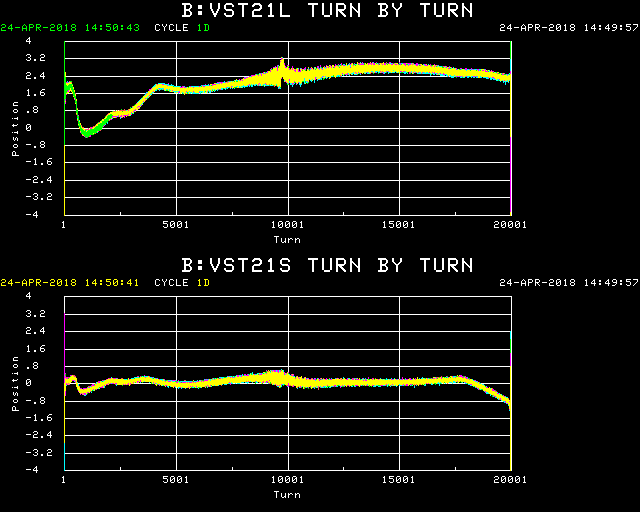
Boards Available

1. 7 Timing boards are functional, 1 not working 1 in transit from manufacturing, 1 waiting for FPGA
2. 28 Transition boards fucntional, 8 waiting to be re-tested.

Measurements at L21







Measurements to Implement

1. Smooth Orbit
2. Raw Mode