Meeting Minutes

Craig C. Drennan

Principle Engineer

AD / Instrumentation

P.O. Box 500, MS 308

Kirk Road and Pine Street  
Batavia, Illinois 60510-50­11 USA

Office: 630.840.2160

[cdrennan@fnal.gov](mailto:cdrennan@fnal.gov)

**Date:** March 26, 2020

**Re:** Meeting Minutes, MTCA.4 Reference Design Introductions

**Meeting Time: 11:00 am to 12:00 pm**

**Meeting Location: ZOOM Meeting**

**Attendees:**

Craig Drennan AD/Instrumentation (Chair)

John Diamond AD/Instrumentation

Peter Prieto AD/Instrumentation

Dennis Nicklaus AD/Instrumentation

Ryan Rivera SCD/DAQ & Electronics

Krzysztof Szczurek SCD/DAQ & Electronics

**Request for Feedback:**

Please send any additions, corrections, rephrasing and/or comments to Craig Drennan. There has been liberal use of paraphrasing in recalling what others have said in the meeting. There may also be some editorializing and introduction of new thoughts that could use some review. Thank You.

**Minutes:**

Introduction

Slides and the minutes are stored on the Accelerator Division DocDB at Beams-doc-8194.

Contact Craig Drennan if you have any trouble accessing the files from this location. For this first meeting I will include slides and minutes as an email attachment.

This meeting was held over ZOOM because of the Shelter-at-Home order implemented by the State of Illinois and the Fermilab management. Members of AD/Instrumentation, AD/Controls and the Scientific Computing Division met to discuss the requirements in the Statement of Work for this MTCA.4 Reference Design Project. Funding had been put into the PIP-II project to prototype and explore the use of mirco-TCA electronics, particularly the revision of the standard, MTCA.4, which provided features requested by the high energy physics community.

AD/Instrumentation has been developing Ethernet transmission of data from their digitizers to get around the bottleneck of transferring data across VME standard backplanes to VME front-end processor. By sending data from the digitizers to a rackmount server over an Ethernet link, the data transfer rate was increased nearly 10 times the rate using VME. Additionally, by sending the data over Ethernet cables and Ethernet switches, the front-end processor no longer needs to reside in the same crate as the digitizers and could be located remotely, and multiple crates could be connected to the same front-end.

A UDP Ethernet protocol was developed by AD/Instrumentation to provide for fast data communications from the FPGA on the digitizers to the Linux based operating system on the front-end processors. This was implemented for BPM DAQ systems for the IOTA experiment and the PIP2IT injector test in 2019-2020.

The reference design for the MTCA.4 DAQ system will provide FPGA code for use in the Xilinx FPGA on the chosen electronics from VadaTech, Inc.. Additionally, software and drivers for the rackmount server front-end will be developed to communicate with the VadaTech equipment. The Statement of Work defines what functions the firmware and software of the reference design will be able to perform.

## Discussion

John Diamond described AD/Instrumentation’s progression of the VME digitizers toward using Ethernet. Ethernet was available on the front of the newer digitizers via an RJ45 connection. Each digitizer is now connected to the front-end through a standard network switch. He described their plans to move from the older MVME5500 processor, in the VME crates, to a 1U rackmount server. The server uses a 10 GbE connection to the Ethernet switch.

The DDCP, UDP protocol was developed to read high speed data (100 Mbytes/s) from the digitizers, read and write registers in the digitizers and provide a method for the digitizers to send an interrupt to the host front-end computer. We want now to see this protocol working with the MTCA.4 equipment.

For the larger BPM and BLM systems, we would have several crates of digitizers delivering data to a host computer that would in turn deliver data to the Control System in the ways the machine users specify.

Peter Prieto said that we would like to have a common system architecture for all our instrumentation to more easily develop and maintain the firmware and software.

Ryan Rivera said that, with the base of firmware that they already have for implementing a UDP Ethernet protocol, they expect to be able to add the DDCP protocol. They could start Krzysztof Szczurek off writing and simulating the firmware without any IP or non-disclosure agreements from VadaTech. Ryan had looked at the DDCP specification and noted that it did not specify how to resolve IP addresses or setting IP addresses in the field. John stated that Instrumentation digitizers were currently using DIP switches on the modules. The VadaTech boards will not have this so addressing will probably need to be handled in the MTCA IPMI (Intelligent Platform Management Interface). Ryan said that we should consider merging the lower level in their UDP Ethernet into the implementation. They have a self-identifying / self-changing IP address protocol built on this lower layer. John said that Instrumentation is definitely interested in what SCD is doing with this.

Craig Drennan said that there is a lot of things that SCD is doing that we would like to learn about. He asked about people’s ability to start working between now and June when the hardware is expected to arrive. John said that he could find some time to start looking into the MCH controller hub and the crate management. Ryan said that they could start considering how to implement the Ethernet in the FPGA and would have a look at the DDCP protocol specification and consider proposing possible additions or modifications. Ryan said that they will start giving Krzysztof things to look at, but Krzysztof may not have a lot of time until he officially arrives in June.

John also mentioned that they are creating a software mockup of the DDCP UDP Ethernet FPGA response of the digitizers. He offered to share this model with SCD.

Ryan has designed an MTCA board and has gone through some of the IPMI setup for turning on power and providing board identification. Ryan, John and Dennis are under the belief that VadaTech supplies tools for managing the IPMI Setup. Craig mentioned that the VadaTech FPGA module had a basic setup for the IPMI and that there was software that ran on the processor in the MCH that provided an interface for setting up the crate management. John concurred that the MCH has a fairly sophisticated processor that can manage the different aspects of the crate, the power supplies and the cooling as well as identifying and managing the modules attached to the crate. VadaTech does have software to interface with this processor. Advanced training, beyond the basics in the reference design, for interfacing and using the features of the MCH is available from VadaTech.

John and Peter raised the question as to where this test hardware would be setup. It was proposed that we set the equipment up in the Transfer Gallery test area and that network access be setup. Ryan agreed that they could work remotely with a Linux node that had a direct JTAG connection to the FPGA to load firmware and run tests remotely. This would be separate from the MTCA crate and John’s Host computer. Ryan said that they are familiar with using Scientific Linux in developing Xilinx FPGAs.

A TCLK connection would be needed for Instrumentation applications but for the demonstration it may not be needed right away. There will be a desire to figure out how to send timing signals across the MTCA backplane, through the MCH. There are also a small number of digital inputs available on the VadaTech modules. It was felt that the LCLK, PIP-II Linac clock system, will be more developed by the time we finish developing the demonstration, reference design with the MTCA.4 equipment.

John mentioned that we will also need a host computer interface to the analog signal conditioning electronics. The analog signal conditioning may be on future MRT rear transition cards in the MTCA crate or in a separate analog crate.

Ryan Rivera expects to design the functions in the FPGA without the implementation of a processor, with everything written in VHDL. He also proposes developing and using open source IP for all of the FPGA logic components. This would include the DDR memory management and the Ethernet interface. Ryan is confident that they can achieve a low latency Ethernet connection building of their existing code and implementing Instrumentations DDCP protocol. Ryan stated that we should work to get the Ethernet interface working as the first goal.

Craig asked people to try and develop the demonstration reference code using either vendor IP or in house, open source IP, but get the demonstration done by September. Further development to the desired configuration can be funded after demonstrating our ability to use the MTCA.4 electronics.

Craig proposed meeting again in two weeks, after people have had time with some of the documentation. We could bring up questions about the documentation, additions or changes to the specification, etc..

Before next meeting

1. Craig will make a list of the documentation we expect everyone to have available.
2. Craig will look into the license issues around the VadaTech reference design IP.
3. Ryan will look at and consider proposing edits to the DDCP Specification.
4. Consider meeting to discuss the DHCP-like method for assigning IP network addresses to the boards.
5. John will pass on information about their software mockup of the FPGA ethernet node.

If you remember something you found important that we should include in these minutes, let me know and I will add it.