Meeting Minutes

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**Date:** April 16, 2020

**Re:** Meeting Minutes, MTCA.4 Reference Design 2nd Meeting

**Meeting Time: 11:00 am to 12:00 pm**

**Meeting Location: ZOOM Meeting**

**Attendees:**

Craig Drennan AD/Instrumentation (Secretary)

John Diamond AD/Instrumentation

Robert Santucci AD/Instrumentation

Peter Prieto AD/Instrumentation

Dennis Nicklaus AD/Controls

Ryan Rivera SCD/DAQ & Electronics

Krzysztof Szczurek SCD/DAQ & Electronics

**Request for Feedback:**

Please send any additions, corrections, rephrasing and/or comments to Craig Drennan. There has been liberal use of paraphrasing in recalling what others have said in the meeting. There may also be some editorializing and introduction of new thoughts that could use some review. Thank You.

**Minutes:**

Introduction

This was the second meeting to discuss the MTCA.4 demonstration and reference design project.

Discussion

Craig Drennan put out, just before the meeting a list of the documentation that everyone should have gotten access to. This included MTCA standards documentation and user manual information for the Vadatech equipment. Craig also had gotten verification from Vadatech that we will always be free to use the IP firmware that comes with the MTCA FPGA module and the MCH control hub, as long as we are using the IP with their products.

Craig reported that the AD division approved money for buying additional MTCA components. We can use this extra equipment as spares and or to expand the scope of our evaluation. The additional components would be the same MRT523 and AMC523, the same MCH, but we would buy a 12-slot crate instead of the 6-slot crate that had been purchased. This would give us the opportunity to evaluate the larger crate which we expect to need in certain applications. The money for this is expected to be available in May.

Ryan Rivera reported that Krzysztof Szczurek had made some progress learning the DDR memory interface. Ryan presented some slides comparing the specification of the DDCP protocol we wish to use for the reference design and features of the OEI (otsdaq Ethernet Interface) that the Scientific Computing Department had design previously.

Noted Differences between

1. Up to this point DIP switches have been used to define ethernet IP addresses on the Instrumentation boards using the DDCP ethernet protocol. Ryan proposed a protocol solution to identifying nodes, particularly since the Vadatech hardware will not have DIP switches. It was agreed that we want to consider something more sophisticated.
2. The MTU, maximum packet size specified in the DDCP is 9000 bytes. Some older ethernet equipment (routers, switches) limit the MTU to 1500 bytes, though newer standards allow for more. SCD’s OEI protocol was written for this limit of 1500 bytes (0 to 180 quad-words).

John Diamond commented that in developing the DDCP protocol they had started with an MTU of 1500 bytes, but in the several trials to get the links data rates up, they had increased the MTU to 9000 bytes. This was done early in the development and perhaps going to 9000 instead of 1500 is not necessary. John suspects that if SCD had good performance with using 1500, then the limit could be successfully set back to 1500. John also noted that the software stack turned out to be the limiting factor, more than the amount of data you can put on the wire.

Ryan said that he prefers to use the MTU of 1500 and points out that the DDCP document has a statement that says the network packets may need to be broken up because of the network switches that are used.

1. The current DDCP default port is expected to be port 65000. Currently OEI is using port 2001. Ryan asked what the origin of this choice was. John replied that the port numbers are arbitrary, and Duane Voy had a reason for choosing a port up in the 60000 range for some Unix convention. Ryan said this difference is not a problem.
2. Ryan noted that the DDCP protocol expects to have a tunable delay between packets on the FPGA transmit side. This is not a feature the OEI protocol has.
3. Ryan noted that the DDCP allows unsolicited requests from the hardware, FPGA server side. This is the implementation of interrupts from the digitizers. The OEI protocol does not do this.

John described our desire to allow the digitizers to alert the host computer (the client) that the asynchronous trigger event has occurred, and data is now available. This is an important feature.

Ryan’s Description of the otsdaq System Ethernet

Ryan stated that the Ethernet logic in the FPGA is implemented completely without soft or hard processors and does not use any proprietary IP. It is written entirely in VHDL/Verilog.

Ryan described the implementation of the ostdaq’s Ethernet controller and the OEI protocol wrapper functions. In his slides he provided these links for the ethernet documentation and the full otsdaq project

<https://cdcvs.fnal.gov/redmine/projects/otsdaq/wiki/OtS_Ethernet_Interface>

<https://otsdaq.fnal.gov>

The slides also provided a link to the design repository on cdcvs.fnal.gov.

Ryan listed several functions built into the Ethernet controller that he recommends for the AD implementation.

1. Settable MAC, IP address and Port number with defaults at power up or reset.
2. The controller handles the reply to any ARP request (Address Resolution Protocol). Ethernet switches and network interface cards will periodically send out ARP requests in order to map out the path to IP addresses on the network.
3. Standard ICMP pings are responded to by the Ethernet controller.
4. The controller ignores, then, anything that is not an ARP, an addressed ICMP ping, or an addressed UDP packet.
5. The controller responds to special Single-Byte UDP packets. The functions for this included a way to change the IP address of a node but was later abandoned for something more robust. It also included a method to retrieve a version number, a way to set addresses for clients to indicate where data was to be sent, and provided for a no-op function that was found to be needed to keep a node from dropping off.
6. Currently the AD Ethernet using the DDCP protocol has not been setup to send data to more than one destination.

Ryan explain features of the OEI protocol wrapper. These features are interesting but are likely different or explained or implemented differently by the DDCP protocol. Ryan did describe how the OEI is setup to have two transmit channels. There is one channel for sending physics data in a burst mode, and a second data channel that is regulated by the receiver of the data. Control data can interrupt the delivery of bursting or physics data. These data channels can also have different destinations.

Ryan’s Proposed Initial Approach and Questions.

Ryan’s proposal for implementing the Ethernet for our MTCA.4 demonstration and reference design is to keep the Ethernet controller they have now but replace the OEI protocol wrapper with the DDCP protocol.

1. Ryan will be looking to map the DDCP “\_feature” to the OEI concept of “internal address space” and map the DDCP “\_index” to the OEI concept of “external address space”.
2. Ryan is considering making the FPGA MAC address, the IP address and the port number a DDCP feature.
3. John and Ryan considered how to change the default IP address when there are several Server nodes (digitizers) on the network that turn on with this same default address. There was a discussion of using MTCA crate functions to power the boards one at a time. There might be an MTCA crate MCH function for configuring the boards in the crate with IP Addresses according to slot.
4. John mentioned that the standard for standalone boards (or any other nodes I suppose – CCD) is DHCP. However, Ryan pointed out that a full implementation of DHCP may be difficult for FPGA and he does not have that implemented with the otsdaq/OEI Ethernet.
5. Ryan mentioned that the boards in the MTCA crate are addressable by slot. His experience has been that related to the powering of each slot.
6. It was proposed that until we have a method in hand, we can simply hard code the addresses of the nodes.

Ryan had some questions.

1. Do we want to consider single byte UDP messages as outline previously?
2. Do we want FPGA transmissions to go to more than one destination? Applications he has seen will have the big pipe, high bandwidth data path going towards one node and the controls being managed by another node. Dennis Nicklaus said that this could be a good thing to have and it was something they found valuable in a previous application of theirs.
3. Do we want operations that index increments towards the count and that do not increment towards the count?
4. We need to learn more about the Vadatech implementation of MTCA and the MCH control hub.

SIDE NOTES:

1. The DDCP protocol does not define everything that needs to be implemented. The ARP protocol and the configuration manager are examples of additional items.
2. We should work to allow SCD to implement the DDCP protocol with their existing otsdaq firmware with as minimal effort as we can arrange. AD software people should consider the things the otsdaq ethernet needs to work. If the otsdaq feature is difficult and unnecessary in our context to implement we could then consider seeing how the otsdaq could be further modified.
3. We want to have non-MTCA stand alone nodes on our network. MTCA nodes may have a configuration manager process to set their IP addresses. Stand alone nodes may need to rely on DIP switches. The DDCP protocol or other protocol used with DDCP in the Instrumentation data network may need to make distinction between how MTCA nodes and other nodes are managed.

Krzysztof Szczurek Notes on DDR IP Using the Vadatech FPGA

Krzysztof Szczurek had been studying ways to implement the DDR memory interface in the Vadatech FPGA. He had studied the information from Vadatech and compared the IP that Vadatech provides for evaluating the DDR memory interface with a standard Xilinx IP for implementing this memory interface.

Krzysztof believes we should use standard Xilinx blocks and had found a Xilinx DMA block that worked with the AXI bus architecture of the Xilinx FPGA. He studied the Xilinx Memory Interface Generator (MIG) application. He was able to take information from the Vadatech implementation and pin assignments and generate the block and a simulation.

It was also determined that the IP from Vadatech would be free to use if we are using it on their boards. Krzysztof will continue with the integration of the blocks needed for the demonstration.

It was felt that by using IP blocks from Xilinx instead of the Vadatech blocks, there would be a more standard solution that could be used with boards other than Vadatech’ s.

Vadatech Delivery of the MTCA.4 Hardware

The delivery of the Vadatech MRT523 ADC rear board, the AMC523 FPGA front board, and the MTCA.4 6 slot crate with the MCH crate control hub is expected in June still. There is a plan, and money, to buy an additional MRT523, an AMC523 and a 12-slot crate with the same MCH as the 6-slot crate. The additional components could be used to expedite the development and provide spares should something unfortunate happen. We believe that the 12-slot crate will not be any different than the 6-slot crate, but will allow us to evaluate the larger crate.

If you remember something you found important that we should include in these minutes, let me know and I will add it.